VSC8244
Data Sheet

Quad 10/100/1000BASE-T PHY with RGMII and RTBI MAC Interfaces

1 General Description

Ideally suited for high port density Gigabit Ethernet switches and routers, or multi-port Network Interface Cards (NICs), Vitesse's VSC8244 integrates four low-power, triple speed (10BASE-T, 100BASE-TX, and 1000BASE-T) Ethernet transceivers in thermally-enhanced, 260-pin plastic Ball Grid Array (BGA).

The VSC8244 physical layer "PHY" IC leverages Vitesse's proprietary 4th generation DSP Technology. Vitesse's highly optimized DSP architecture yields industry leading performance at less than 640mW per port, supporting 1000BASE-T with respect to all worst case impairments (NEXT, FEXT, Echo, and system noise sources).

Each of the four independent triple-speed transceivers features pin-efficient RGMII and RTBI compliant MAC interfaces. On-chip RGMII/RTBI series termination resistors simplify board design challenges by improving signal integrity and completely eliminating dozens of external series termination resistors on the receive side of the MAC interface. In addition, the VSC8244 integrates, for the first time in the industry, all copper media side line termination resistors.

To enable maximum network management feedback to the host system and the user, the VeriPHY® Link Management and Cable Diagnostics Suite can be used with the device. VeriPHY provides extensive network and cable plant operating and status information, such as the cable length, termination status, and open/short fault location. VeriPHY integrates with NIC or switch software to greatly simplify Gigabit Ethernet network deployment and management by providing the functionality equivalent to a hand-held cable tester.

2 System Diagrams

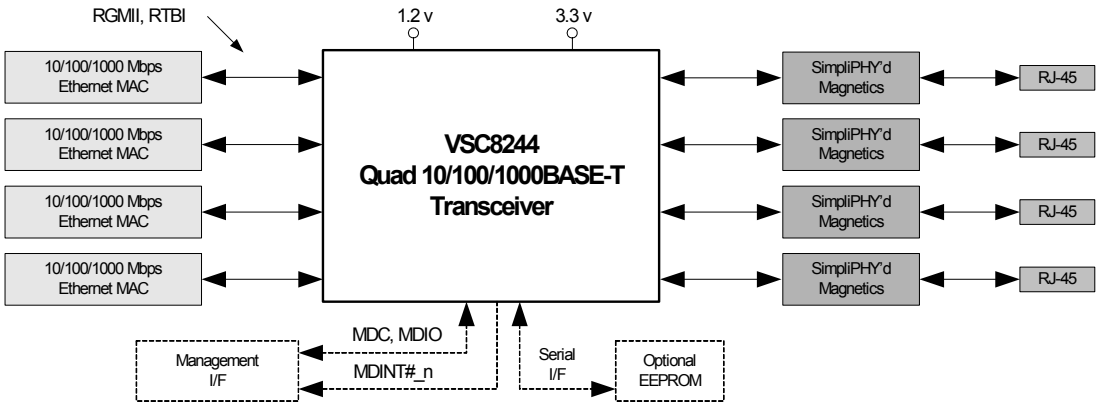

Figure 1. VSC8244 System Diagram

3 Features / Benefits

Features	Benefits
• Quad, low power, 10/100/1000BASE-T in a 19mm HS-BGA package	• Catalyzes market for low-cost & high density LAN, WAN, SAN, & MAN switches
• Lowest power consumption in the industry at less than 640mW/port (1000BASE-T mode)	• Eliminates heatsinks and fans for Gigabit to the desktop LAN switches
• Supports PICMG 2.16 and 3.0 Ethernet backplanes at less than 500 mW/port	• Lowest power mode reduces supply costs
• Patented, low EMI line driver with integrated line side termination resistors	• Removes 12 passive components per PHY*, reducing PCB area & cost by 50% • Saves up to 50% on magnetic module cost with SimpliPHY'd magnetics • Enables magnetic-less PICMG backplane designs
• Supports RGMII v1.3 (2.5V & 3.3V) & v2.0 (1.5V HSTL)	• Compatible with a wide variety of parallel I/F switch ICs
• User-programmable RGMII timing compensation	• Simplifies PCB layout; eliminates PCB trombones
• Compliant with IEEE 802.3 (10BASE-T, 100BASE-TX, 1000BASE-T) specifications	• Ensures seamless deployment throughout copper networks with industry's highest tolerance to noise and substandard cable plants
• >10kB jumbo frame support with programmable synchronization FIFOs	• Provides for maximum jumbo frame sizes in custom SAN and LAN systems
• Five Direct drive LEDs per port with on-chip filtering or serial LED interface option	• Eliminates external components and EMI issues
• Three user configuration options: 1) optional serial EEPROM, 2) hardware configuration pins, or 3) Serial Management Interface (SMI)	• Offers design engineer a solution to fit any unmanaged or managed system requirement
• Full suite of BIST, near-end, and far-end loopback modes	• Simplifies comprehensive in-system test to ensure highest product quality
• VeriPHY® cable diagnostics	• Pin-points potential cable plant problems by providing equivalent diagnostic capabilities of a sophisticated hand-held cable tester
• Automatic detection and correction of cable pair swaps, pair skew and pair polarity, along with HP Auto MDI/MDI-X crossover function	• Compatible with 1st generation 1000BASE-T PHYs. • Supports Auto MDI/MDI-X even when Autonegotiation is disabled
• Manufactured in advanced 0.13µm, 3.3V/1.2V digital CMOS process	• Most cost effective technology eliminates more expensive analog process variants

* or, 576 components for a 48-port switch

4 Applications

- High Port Density 10/100/1000BASE-T Switches
- Workgroup LAN Switches & Routers
- Backplane Applications such as PICMG 2.16, 3.0
- Gigabit Ethernet-based SAN, NAS, and MAN Systems
- High Performance Workstations & Multi-Port Server NICs

5 Device Block Diagram

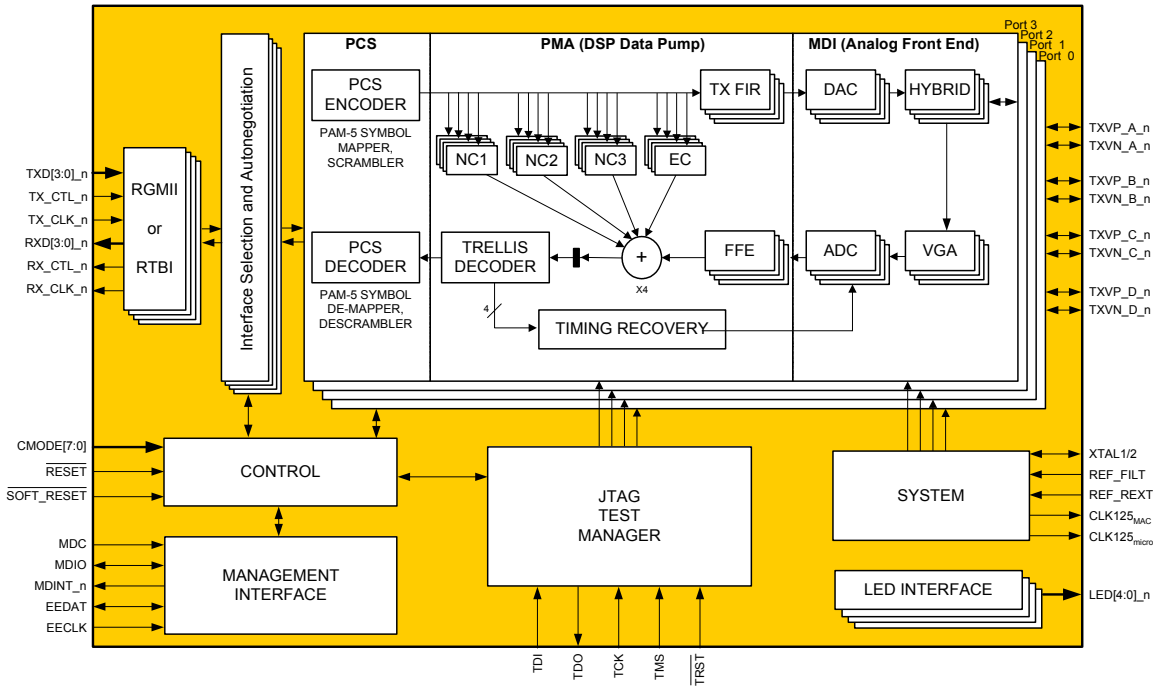

Figure 2. VSC8244 Block Diagram[1]

[1] n = port number (0, 1, 2, 3)

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6 Relevant Specifications & Documentation

The VSC8244 conforms to the following specifications. Please refer to these documents for additional information.

Table 1. VSC8244 Relevant Specifications

Specification - Revision	Description
IEEE 802.3-2002	Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications. IEEE 802.3-2002 consolidates and supersedes the following specifications: 802.3ab (1000BASE-T), 802.3u (Fast Ethernet), with references to ANSI X3T12 TP-PMD standard (ANSI X3.263 TP-PMD).
IEEE 1149.1-1990	Test Access Port and Boundary Scan Architecture[1]. Includes IEEE Standard 1149.1a-1993 and IEEE Standard 1149.1b-1994.
JEDEC EIA/JESD8-5	2.5V±0.2V (Normal Range), and 1.8V to 2.7V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits.
JEDEC JESD22-A114-B	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM). Revision of JESD22-A114-A.
JEDEC JESD22-A115-A	Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM). Revision of EIA/JESD22-A115.
JEDEC EIA/JESD78	IC Latch-Up Test Standard.
MIL-STD-883E	Miltary Test Method Standard for Microcircuits.
RGMII Specification - v1.3, v2.0	Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Devices (per Hewlett Packard). Includes both RGMII and RTBI standards.
PICMG 2.16	IP Backplane specification for CompactPCI v2.16.
Advanced TCA™ Base PICMG 3.0	IP Backplane specification for CompactPCI v3.0.
Cisco InLIne Power Detection Algorithmn	Cisco Sytems InLine Power Detection: http://www.cisco.com/en/US/products/hw/phones/ps379/products_tech_note09186a00801189b5.shtml

[1] Often referred to as the “JTAG” test standard.

7 VSC8244 Differences vs. VSC8224/VSC8234 Devices

The VSC8244 is one of three, quad port PHY devices featuring Vitesse's proprietary fourth-generation DSP technology. It provides parallel RGMII/RTBI interfaces and 10/100/1000BASE-T Category-5, Unshielded Twisted Pair (UTP) copper media interfaces. The VSC8234 features serial SGMII/SerDes MAC interfaces with Category-5 UTP media interfaces. The VSC8224 is the dual media capable device featuring RGMII/RTBI parallel MAC interfaces with support for both 10/100/1000BASE-T and 1000BASE-X media interfaces.

The following table summarizes the MAC and media interfaces supported by the VSC8244, the VSC8234, and the VSC8244 quad-port PHY:

Table 2. VSC8224/VSC8234/VSC8244 MAC / Media Interface Support Options

Device #	MAC Interface	Media Interface	Package Options	Full Part Number
VSC8224	RGMII / RTBI	CAT-5	260-pin HS-PBGA	VSC8224HG
	RGMII / RTBI	SerDes (1000Base-X)		
VSC8234	SGMII (4 or 6 pin)	CAT-5	260-pin HS-PBGA	VSC8234HG
	SerDes (1000Base-X)	CAT-5		
VSC8244	RGMII / RTBI	CAT-5	260-pin HS-PBGA	VSC8244HG

7.1 VSC8244 Functional Differences

The VSC8244 is a functional subset of the VSC8224 in that it provides all the same features except for the following:

- No media side SerDes interfaces for supporting 1000BASE-X (fiber).
- Differences in the CMODE configurations settings as certain functions in the VSC8224 relating to the serial interface are not present in the VSC8244. This includes several MAC interfaces, SIGDET direction setting, and SerDes termination impedance setting

7.2 VSC8244 Register Differences

The VSC8244 is the exact register map equivalent to the VSC8224's register map with the following exceptions:

- Register 3: Device number indication changes to VSC8244.
- Register 23:
  - Bit 15 is Reserved and must be set to 0.
  - Bits 14:12 less modes are present. Only modes involving RGMII-CAT5 and RTBI-CAT5 exist in the VSC8244.
- Register 24: TXFIFO settings only affect RGMII as opposed to SerDes and SGMII as in the VSC8224.
- Register 25 & 26: Bit 4 for the Auto-Media Sense (AMS) indication condition is not available.
- Register 16E: Only bits 2:0 (Remote Fault bit settings) are relevant on the VSC8244.
- Register 20E: Bits 7:5 related to AMS and SerDes termination impedance for the VSC8224 are not present in the VSC8224.

7.3 VSC8244 Pinout Differences

The 260-pin HS-PBGA packages between the VSC8224HG and the VSC8244HG are the exact same (pin-for-pin compatible), except for the following pins:

The following pins are NC on the VSC8244HG 260-pin HS-PBGA:

- Pins T1, M1, H1, D1, U1, N1, J1, E1 -- TDP/N_[3:0] signals
- Pins R1, L1, G1, C1, P1, K1, F1, B1 -- RDP/N_[3:0] signals
- Pins R2, L2, G2, C2, T2, M2, H2, D2 -- RCP/N_[3:0] signals
- Pins E2, J2, N2, U2 -- SIGDET_[3:0] signals

8 Data Sheet Conventions

Conventions used throughout this data sheet are specified in the following table.

Table 3. Data Sheet Conventions

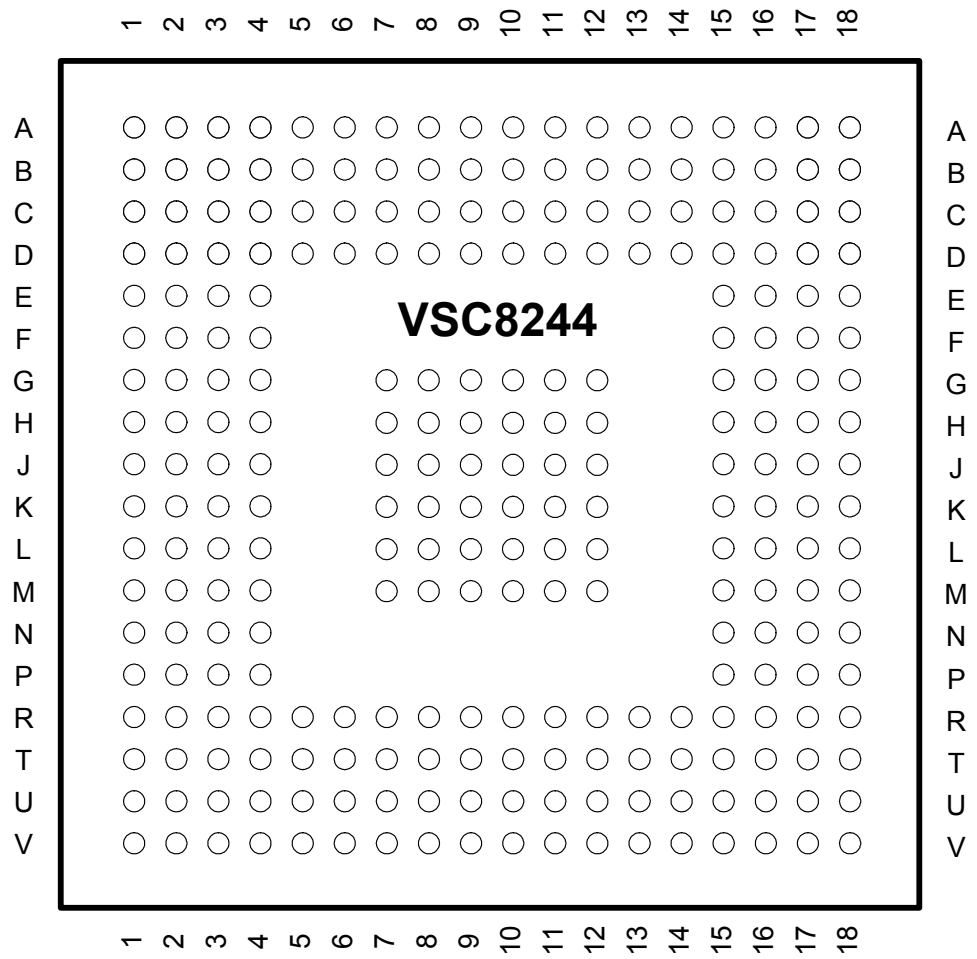
Convention	Syntax	Examples	Description
Register number	RegisterNumber.Bit or RegisterNumber.BitRange	23.10 23.12:10	Register 23 (address 17h), bit 10. Register 23 (address 17h), bits 12, 11, and 10.
Extended Page Register number	RegisterNumberE.Bit or RegisterNumberE.BitRange	23E.10 23E.12:10	Extended Register 23 (address 17h), bit 10. Extended Register 23 (address 17h), bits 12, 11, and 10.
Signal name (active high)	SIGNALNAME[1]	PLLMODE	Signal name for PLLMODE.
Signal name (active low)	$\overline{\text{SIGNALNAME}}$[1]	$\overline{\text{RESET}}$	Active low reset signal.
Signal bus name	BUSNAME[MSB:LSB][1]	CMODE[4:0][2]	CMODE configuration bits 4, 3, 2, 1, and 0.
PHY port number	_n	_3	Denotes a specific PHY port #3. n= {3 || 2 || 1 ||0}.
PHY-specific port signal	SIGNALNAME_n[1]	RX_CTL_3	RX_CTL signal for PHY port 3[3].
Signal bus for a specific PHY port	SIGNALNAME[MSB:LSB]_n[1]	RXD[3:0]_3	Receive data bus, bits 3through 0, for PHY port #3[3].

[1] All signal names are in all CAPITAL LETTERS.
[2] CMODE is common to entire device.
[3] RXD signals are unique to each PHY.

9 Package Pin Assignments & Signal Descriptions

9.1 260 HS-PBGA Package Ball Diagram

For complete specifications, refer to Section 26: “Packaging Specifications”.



260 HS-PBGA
1.0mm Ball Pitch (19mm body size)
(Top View)

Figure 3. 260 HS-PBGA Package Ball Diagram
(View from top of package with underlying BGA ball positions superimposed)

9.2 BGA Ball to Signal Name Cross Reference (LEFT side)

	1	2	3	4	5	6	7	8	9
A	LED[4]_3	LED[0]_2	TXVPD_3	TXVPC_3	TXVPB_3	TXVPA_3	TXVPD_2	TXVPC_2	TXVPB_2
B	NC	LED[1]_2	TXVND_3	TXVNC_3	TXVNB_3	TXVNA_3	TXVND_2	TXVNC_2	TXVNB_2
C	NC	NC	LED[2]_2	LED[3]_2	LED[4]_2	NC	NC	VDD33	REF_REXT
D	NC	NC	LED[3]_3	VDD33	VDD33	VDD33	VSSS	VSSS	VDD33
E	NC	NC	LED[2]_3	VDD12					
F	NC	VSSS	LED[1]_3	VDD12					
G	NC	NC	LED[0]_3	VSSS			VSSS	VSSS	VSSS
H	NC	NC	VDD12	VDDDIG			VSSS	VSSS	VSSS
J	NC	NC	VDD12	VDDDIG			VSSS	VSSS	VSSS
K	NC	VSSS	VSSS	VSSS			VSSS	VSSS	VSSS
L	NC	NC	VSSS	VDD33			VSSS	VSSS	VSSS
M	NC	NC	VDD12	VSSS			VSSIO	VSSIO	VSSIO
N	NC	NC	VDD12	VSSS					
P	NC	VSSS	VSSS	VDDDIG					
R	NC	NC	VDD12	VDDDIG	$VDDIO_{MAC}$	$VDDIO_{MAC}$	$VDDIO_{MAC}$	TXREF_2	$VDDIO_{MAC}$
T	NC	NC	TXREF_3	RXD[2]_3	TX_CLK_3	TXD[2]_3	RX_CLK_2	RXD[2]_2	TX_CLK_2
U	NC	NC	RX_CTL_3	RXD[1]_3	TX_CTL_3	TXD[1]_3	RX_CTL_2	RXD[1]_2	TX_CTL_2
V	NC	RX_CLK_3	RXD[3]_3	RXD[0]_3	TXD[3]_3	TXD[0]_3	RXD[3]_2	RXD[0]_2	TXD[3]_2
	1	2	3	4	5	6	7	8	9

Figure 4. 260-Pin HS-PBGA (19mm) Signal Map (TOP LEFT side of package)

9.3 BGA Ball to Signal Name Cross Reference (RIGHT side)

10	11	12	13	14	15	16	17	18	
TXVPA_2	TXVPD_1	TXVPC_1	TXVPB_1	TXVPA_1	TXVPD_0	TXVPC_0	TXVPB_0	TXVPA_0	A
TXVNA_2	TXVND_1	TXVNC_1	TXVNB_1	TXVNA_1	TXVND_0	TXVNC_0	TXVNB_0	TXVNA_0	B
REF_FILT	VSSS	VSSS	VSSS	VSSS	NC	CMODE[7]	CMODE[6]	CMODE[5]	C
VDD33	VDD33	VDD33	VDD33	VDD12	VDD12	CMODE[4]	XTAL1 or REFCLK	XTAL2	D
					NC	CMODE[3]	CMODE[2]	CMODE[1]	E
					VDD33	CMODE[0]	LED[0]_1	LED[1]_1	F
VSSS	VSSS	VSSS			VDD33	LED[2]_1	LED[3]_1	LED[4]_1	G
VSSS	VSSS	VSSS			VDDDIG	LED[0]_0	LED[1]_0	LED[2]_0	H
VSSS	VSSS	VSSS			VDDDIG	TDI	LED[3]_0	LED[4]_0	J
VSSS	VSSS	VSSS			$VDDIO_{ctl}$	TDO	TCK	TMS	K
VSSS	VSSS	VSSS			$VDDIO_{micro}$	$\overline{TRST}$	EECLK or PLLMODE	EEDAT	L
VSSIO	VSSIO	VSSIO			VSSIO	$\overline{RESET}$	$\overline{SOFT\_RESET}$	OSCEN or $CLK125_{micro}$	M
					VSSS	MDINT_1	MDINT_2	MDINT_3	N
					VSSS	MDC	MDIO	MDINT_0	P
TXREF_1	$VDDIO_{MAC}$	$VDDIO_{MAC}$	TXREF_0	VDDDIG	VDDDIG	VDD33	$CLK125_{MAC}$	MICROREF	R
TXD[2]_2	RX_CLK_1	RXD[0]_1	TXD[3]_1	TXD[0]_1	RXD[3]_0	RXD[0]_0	TXD[3]_0	TXD[0]_0	T
TXD[1]_2	RX_CTL_1	RXD[1]_1	TX_CLK_1	TXD[1]_1	RX_CTL_0	RXD[1]_0	TX_CTL_0	TXD[1]_0	U
TXD[0]_2	RXD[3]_1	RXD[2]_1	TX_CTL_1	TXD[2]_1	RX_CLK_0	RXD[2]_0	TX_CLK_0	TXD[2]_0	V
10	11	12	13	14	15	16	17	18	

Figure 5. 260-Pin HS-PBGA (19mm) Signal Map (TOP RIGHT side of package)

9.4 Signal Type Descriptions

Table 4. Signal Type Descriptions

Symbol	Signal Type	Description
I	Digital Input	Standard digital input signal. No internal pull-up or pull-down.
I_{PU}	Digital Input with Pull-up	Standard digital input. Includes on-chip 100kΩ pull-up to VDDIO.
I_{PD}	Digital Input with Pull-down	Standard digital input. Includes on-chip 100kΩ pull-down to VSSIO.
O_{ZC}	Impedance Controlled Output	50Ω integrated (on-chip) source series terminated, digital output signal. Used primarily for timing-sensitive MAC I/F and 125MHz clock output pins, in addition to high speed manufacturing test mode pins.
I_{PD}/O	Digital Bidirectional	Tristate-able, digital input and output signal. Includes on-chip 100kΩ pull-down to VSSIO.
OD	Digital Open Drain Output	Open drain digital output signal. Must be pulled to VDDIO through an external pull-up resistor.
A_{DIFF}	Analog Differential	Analog differential signal pair for twisted pair interface.
A_{BIAS}	Analog Bias	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network, as shown in Section 10: “System Schematics”.
I_A	Analog Input	Analog input for sensing variable voltage levels.
OS	Open Source	Open source digital output signal. Must be pulled to GND through an external pull-down resistor.
V_{REF}	Voltage Reference Input	Voltage Reference input pins required for VDDIO HSTL mode.
I_{PUJTAG}	JTAG Input	JTAG input pin. Includes on-chip pullup to $VDDIO_{CTL}$. These pins are 5V tolerant when $VDDIO_{CTL}$ = 3.3V. For $VDDIO_{CTL}$ = 2.5V, these pins are up to 4.7V tolerant.
O_{CRYST}	Crystal Output	Crystal clock output pin. If not used, leave unconnected.
NC	No Connect	No connect signal. Must be left floating.

9.5 MAC Transmit Interface (MAC TX) Pins

The following pins are used for connecting to a parallel data bus MAC via the industry-standard RGMII and RTBI interfaces.

Table 5. MAC TX Signal Descriptions

HSBGA Ball #	Signal Name MAC Interface Modes		Type	Description
	RGMII	RTBI		
V5, T6, U6, V6 V9, T10, U10, V10 T13, V14, U14, T14 T17, V18, U18, T18	TXD[3:0]_3 TXD[3:0]_2 TXD[3:0]_1 TXD[3:0]_0	TXD[3:0]_3 TXD[3:0]_2 TXD[3:0]_1 TXD[3:0]_0	I_{PD}	**Multiplexed Transmit Data Nibbles (RGMII mode)** Bits [3:0] are synchronously input on the rising edge of TX_CLK_n, and bits [7:4] on the falling edge of TX_CLK_n. **Multiplexed Transmit Data Nibbles (RTBI mode)** Bits [3:0] are synchronously input on the rising edge of TX_CLK_n, and bits [8:5] on the falling edge of TX_CLK_n.
U5 U9 V13 U17	TX_CTL_3 TX_CTL_2 TX_CTL_1 TX_CTL_0	TXD[4]_3 TXD[4]_2 TXD[4]_1 TXD[4]_0	I_{PD}	**Transmit Enable, Transmit Error Multiplexed Input (RGMII mode)** In RGMII mode, this input is sampled by the PHY on opposite edges of TX_CLK_n to indicate two transmit conditions of the MAC: 1) on the rising edge of TX_CLK_n, this input serves as TXEN, indicating valid data is available on the TD input data bus. 2) on the falling edge of TX_CLK_n, this input signals a transmit error from the MAC, based on a logical derivative of TXEN and TXER, per RGMII specification Version 2.0. **Multiplexed Transmit Data (RTBI mode)** Bit [4] is synchronously input on the rising edge of TX_CLK_n, and bit [9] on the falling edge of TX_CLK_n.
T5 T9 U13 V17	TX_CLK_3 TX_CLK_2 TX_CLK_1 TX_CLK_0	TX_CLK_3 TX_CLK_2 TX_CLK_1 TX_CLK_0	I_{PD}	**Transmit Clock Input (RGMII mode)** The transmit clock shall be either a 125MHz or 25MHz (for 1000Mb or 100Mb modes, respectively), with a +/-50ppm tolerance. If left unconnected, these pins will require a pull-down resistor to ground.

9.6 MAC Receive Interface (MAC RX) Pins

All output pins for the MAC interface include impedance-calibrated, tristateable output drive capability.

Table 6. MAC RX Signal Descriptions

HSBGA Ball #	Signal Name MAC Interface Modes		Type	Description
	RGMII	RTBI		
V3, T4, U4, V4 V7, T8, U8, V8 V11, V12, U12, T12 T15, V16, U16, T16	RXD[3:0]_3 RXD[3:0]_2 RXD[3:0]_1 RXD[3:0]_0	RXD[3:0]_3 RXD[3:0]_2 RXD[3:0]_1 RXD[3:0]_0	O_{ZC}	**Multiplexed Receive Data Nibble (RGMII mode only)** Bits [3:0] are synchronously output on the rising edge of RX_CLK_n, and bits [7:4] on the falling edge of RX_CLK_n. **Multiplexed Receive Data Nibbles (RTBI mode)** Bits [3:0] are synchronously output on the rising edge of RX_CLK_n, and bits [8:5] on the falling edge of RX_CLK_n.
V2 T7 T11 V15	RX_CLK_3 RX_CLK_2 RX_CLK_1 RX_CLK_0	RX_CLK_3 RX_CLK_2 RX_CLK_1 RX_CLK_0	O_{ZC}	**Receive Clock Output (RGMII and RTBI modes)** Receive data is sourced from the PHY synchronously on the rising edge of RX_CLK_n and is the recovered clock from the media.
U3 U7 U11 U15	RX_CTL_3 RX_CTL_2 RX_CTL_1 RX_CTL_0	RXD[4]_3 RXD[4]_2 RXD[4]_1 RXD[4]_0	O_{ZC}	**Multiplexed Receive Data Valid / Receive Error Output (RGMII mode only).** In RGMII mode, this output is sampled by the MAC on opposite edges of RX_CLK_n to indicate two receive conditions from the PHY: 1) on the rising edge of RX_CLK_n, this output serves as RXDV, signaling valid data is available on the RD input data bus, 2) on the falling edge of RX_CLK_n, this output signals a receive error from the PHY, based on a logical derivative of RXDV and RXER, per RGMII specification Version 2.0. **Multiplexed Receive Data (RTBI mode)** Bit [4] is synchronously output on the rising edge of RX_CLK_n, and bit [9] on the falling edge of RX_CLK_n.

9.7 Twisted Pair Interface Pins

Table 7. Twisted Pair Interface Pins

HSBGA Ball #	Signal Name	Type	Description
A6 A10 A14 A18	TXVPA_3 TXVPA_2 TXVPA_1 TXVPA_0	A_{DIFF}	**TX/RX Channel "A" Positive Signal** Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the "A" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1. See System Schematic.
B6 B10 B14 B18	TXVNA_3 TXVNA_2 TXVNA_1 TXVNA_0	A_{DIFF}	**TX/RX Channel "A" Negative Signal** Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the "A" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2. See System Schematic.
A5 A9 A13 A17	TXVPB_3 TXVPB_2 TXVPB_1 TXVPB_0	A_{DIFF}	**TX/RX Channel "B" Positive Signal** Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the "B" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3. See System Schematic.
B5 B9 B13 B17	TXVNB_3 TXVNB_2 TXVNB_1 TXVNB_0	A_{DIFF}	**TX/RX Channel "B" Negative Signal** Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the "B" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6. See System Schematic.
A4 A8 A12 A16	TXVPC_3 TXVPC_2 TXVPC_1 TXVPC_0	A_{DIFF}	**TX/RX Channel "C" Positive Signal** Positive differential signal connected to the positive primary side of the transformer. This pin signals forms the positive signal of the "C" data. In 1000Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10M/100M modes). See System Schematic.
B4 B8 B12 B16	TXVNC_3 TXVNC_2 TXVNC_1 TXVNC_0	A_{DIFF}	**TX/RX Channel "C" Negative Signal** Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the "C" data channel. In 1000Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10M/100M modes). See System Schematic.
A3 A7 A11 A15	TXVPD_3 TXVPD_2 TXVPD_1 TXVPD_0	A_{DIFF}	**TX/RX Channel "D" Positive Signal** Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the "D" data channel. In 1000Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10M/100M modes). See System Schematic.
B3 B7 B11 B15	TXVND_3 TXVND_2 TXVND_1 TXVND_0	A_{DIFF}	**TX/RX Channel "D" Negative Signal** Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the positive signal of the "D" data channel. In 1000Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10M/100M modes). See System Schematic.

9.8 Serial Management Interface Pins (IEEE SMI)

Table 8. Serial Management Interface Pins

HSBGA Ball	Signal Name	Type	Description
P16	MDC	I	**Management Data Clock** A 0 to 12.5MHz reference input is used to clock serial MDIO data into and out of the VSC8244. The expected nominal frequency is 2.5MHz, as specified by the IEEE standard. This clock is typically asynchronous with respect to the PHY's transmit or receive clock.
P17	MDIO	OD	**Management Data I/O** MDIO configuration and status data is exchanged on this pin bidirectionally between the PHY and the Station Manager, synchronously to the rising edge of MDC. This signal normally requires a 1.5kΩ to 2kΩ external pull-up resistor at the Station Manager. The value of the pull-up resistor depends on the MDC clock frequency and the maximum capacitive load on the MDIO pin.
P18 N16 N17 N18	MDINT_0 MDINT_1 MDINT_2 MDINT_3	OS/ OD	**Management Interrupt Outputs** These output signals indicate a change in each of the four PHY's link operating conditions for which a station manager must interrogate to determine further information. Upon reset or powerup, the VSC8244 will automatically configure these pins as active-low (open drain) or active-high (open source) based on the polarity of an external resistor connection. For active-low configuration, tie each MDINT_n pin to VDD33 through an external 10kΩ pull-up resistor. For active-high configuration, tie each MDINT_n pin to GND through an external 10kΩ pull-down resistor. If only one MDINT_n signal is desired for all four PHYs, these pins can be tied together on the PCB in a wired-OR configuration with only a single pull-up or pull-down resistor.

9.9 Serial EEPROM Interface Pins

Table 9. Serial EEPROM Interface Pins

HSBGA Ball	Signal Name	Type	Description
L18	EEDAT	I_{PD}/O	**EEPROM Serial Data I/O** The optional EEPROM interface can be used to allow VSC8244 operating mode and configuration data to be read from an external EEPROM. (The EEPROM can also be written if desired.) EEPROM data is synchronously exchanged, bi-directionally, between the VSC8244 and the external EEPROM. Data is clocked from the VSC8244 on the falling edge of EECLK, and into the VSC8244 on the rising edge of EECLK as defined by the ATMEL "AT24CXXX" type EEPROMs. This pin should be connected to the SDA pin of the EEPROM. The VSC8244 determines that an external EEPROM is present by monitoring the EEDAT pin at power-up or when $\overline{\text{RESET}}$ is de-asserted: if EEDAT has a 4.7k external pull-up resistor, the VSC8244 assumes an EEPROM is present. The EEDAT pin can be left floating or grounded to indicate no EEPROM.
L17	EECLK or PLLMODE	I_{PD}/ O_{ZC}	**EECLK - Serial EEPROM Clock Output** This output is the clock line of the two-wire, serial EEPROM interface. The VSC8244 drives this line at a 50 kHz rate on reset. When accessed through the MII registers, this line is driven at a 100kHz rate. This pin should be connected to the SCL pin of the EEPROM. **PLLMODE - PLLMODE - PLL Mode Select Input** PLLMODE is sampled during the device power-up sequence or in reset. When PLLMODE is high, the VSC8244 expects a 125MHz clock input as the PHY's reference clock. When pulled low (default), a reference clock of 25MHz is expected from either an external crystal or a clock reference input. This pin is internally pulled down with a 100k resistor.

9.10 Configuration and Control Pins

Table 10. Configuration and Control Pins

HSBGA Ball	Signal Name	Type	Description
F16 E18 E17 E16 D16 C18 C17 C16	CMODE0 CMODE1 CMODE2 CMODE3 CMODE4 CMODE5 CMODE6 CMODE7	I_A	**Hardware Chip Mode Select** The CMODE inputs are used for hardware configuration of the various operating modes of the VSC8244. Each pin has multiple settings, each of which is established by an external 1% resistor tied to GND or VDD33. See Section 22.3: “CMODE Pin Configuration” for details on configuring the VSC8244 with the CMODE pins.
M16	$\overline{\text{RESET}}$	I_{PU}	**Hardware Chip Reset** $\overline{\text{RESET}}$ is an active low input, which powers down all of the internal reference voltages and the PLL, and resets all internal logic, including the DSPs, PLLs and the MII Management Register bits are set to their default states. Hardware reset is distinct from Software reset which only resets the standard MII Registers.
M17	$\overline{\text{SOFT\_RESET}}$	I_{PU}	**Soft Reset** $\overline{\text{SOFT\_RESET}}$ is an active low input, which places the VSC8244 in a low power state. Although the device is powered down; non-volatile, serial management interface registers retain their values.

9.11 System Clock Interface Pins

Table 11. System Clock Interface Pins

HSBGA Ball	Signal Name	Type	Description
R17	$CLK125_{MAC}$	O_{ZC}	**Reference Clock Output for MAC** This pin serves as a 125MHz reference clock output, which can be used to drive a MAC or other external device. $CLK125_{MAC}$ is powered by the $VDDIO_{MAC}$ supply. This 125MHz clock output pin is enabled by default, but can be disabled via an MII register setting.
M18	OSCEN or $CLK125_{micro}$	I_{PD}/O_{ZC}	**OSCEN - Oscillator Enable** OSCEN is sampled on the rising edge of $\overline{RESET}$ to determine if the on-chip oscillator is enabled, or an external clock is to be used. When tied high through an external 10k pull-up resistor, the oscillator is enabled, allowing operation with an external 25MHz crystal. If OSCEN is tied low (or left floating), the oscillator circuit is disabled and the device must be supplied with either a 25MHz or 125MHz clock input to REFCLK (see EECLK or PLLMODE pin description for more details). **$CLK125_{micro}$ - Reference Clock Output for Microprocessor** This pin serves as a 125MHz or 4MHz reference clock output, which can be used to drive a Microprocessor or other external device. $CLK125_{micro}$ is powered by the $VDDIO_{micro}$ supply. This 125MHz or 4MHz clock output pin is disabled by default, but can be enabled via an MII register setting.
D17	XTAL1 or REFCLK	I	**XTAL1 - Crystal Oscillator Input** If enabled by OSCEN high, a 25MHz parallel resonant crystal, with +/-50ppm frequency tolerance, should be connected across XTAL1 and XTAL2. 33pF capacitors should be connected from XTAL1 and XTAL2 to ground. PLLMODE should be left floating (or pulled low) on reset when a 25MHz crystal is used. **REFCLK - PHY Reference Clock Input** If enabled by OSCEN low, the reference input clock can either be a 25MHz (PLLMODE is low) or 125MHz (PLLMODE is high) reference clock, with a +/-50ppm frequency tolerance. See EECLK or PLLMODE pin description for more details.
D18	XTAL2	O_{CRYST}	**Crystal Output** 25MHz parallel resonant crystal oscillator output. 33pF capacitors should be connected from both XTAL1 and XTAL2 to ground when using a crystal. PLLMODE should be left floating (or tied low) on reset when using the 25MHz crystal. If not using a crystal, this output pin can be left floating if driving XTAL1/REFCLK with a reference clock.

9.12 LED Interface Pins

Table 12. LED Interface Pins

HSBGA Ball	Signal Name	Type	Description
A1, D3, E3, F3, G3 C5, C4, C3, B2, A2 G18, G17, G16, F18, F17 J18, J17, H18, H17, H16	LED[4:0]_3 LED[4:0]_2 LED[4:0]_1 LED[4:0]_0	O_{ZC}	**LED - Direct-Drive LED Outputs** After reset, these pins serve as the direct drive, low EMI, LED driver output pins that can indicate individual status per pin or can be configured to output a serial data stream. All LEDs are active-low and are powered by the VDD33 power supply. The function of each LED pin is configured either through CMODE hardware configuration pins (see Section 22.3: "CMODE Pin Configuration") or through MII Register 27.

9.13 JTAG Test Access Port Pins

Table 13. JTAG TAP Signal Descriptions

HSBGA Ball #	Signal Name	Type	Description
J16	TDI	I_{PUJTAG}	**JTAG Test Data Serial Input Data**. Serial test pattern data is scanned into the device on this input pin, which is sampled with respect to the rising edge of TCK. This pin should be tied high during normal chip operation.
K16	TDO	O_{ZC}	**JTAG Test Data Serial Output Data**. Serial test data from the VSC8244 is driven out of the device on the falling edge of TCK. This pin should be left floating during normal chip operation.
K18	TMS	I_{PUJTAG}	**JTAG Test Mode Select**. This input pin, sampled on the rising edge of TCK, controls the TAP (Test Access Port) controller's 16-state, instruction state machine. This pin should be tied high during normal chip operation.
K17	TCK	I_{PUJTAG}	**JTAG Test Clock**. This input pin is the master clock source used to control all JTAG test logic in the device. This pin should be tied high or left floating during normal chip operation.
L16	$\overline{\text{TRST}}$	I_{PUJTAG}	**JTAG Reset**. This active low input pin serves as an asynchronous reset to the JTAG TAP controller's state machine. As required by the JTAG standard, this pin includes an integrated on-chip pull-up resistor. Because of the internal pull-up, if the JTAG controller on the printed circuit board does *not* utilize the $\overline{\text{TRST}}$ signal, then the device will still function correctly when the $\overline{\text{TRST}}$ pin is left unconnected on the board. Alternatively, if the JTAG port of the VSC8244 is *not* used on the printed circuit board, then this pin should be tied to ground (VSSIO) with a 0 ohm - 4.7k ohm pull-down resistor.

9.14 Analog Bias Pins

Table 14. Analog Bias Pins

HSBGA Ball	Signal Name	Type	Description
C9	REF_REXT	A_{BIAS}	**REF_REXT - Reference External Resistor** Bias pin connects through external 2kΩ (1%) resistor to analog ground.
C10	REF_FILT	A_{BIAS}	**REF_FILT - Reference Filter** Filter internal reference through external 1µF (±10%) capacitor to analog ground.

9.15 HSTL Voltage Reference Pins

Table 15. HSTL Voltage Reference Pins

HSBGA Ball	Signal Name	Type	Description
T3 R8 R10 R13	TXREF_3 TXREF_2 TXREF_1 TXREF_0	V_{REF}	If $VDDIO_{MAC}$ = 1.5V : HSTL voltage reference level from MAC If $VDDIO_{MAC}$ = 2.5V or 3.3V : Tie to GND.
R18	MICROREF	V_{REF}	If $VDDIO_{micro}$ = 1.5V : HSTL voltage reference level from micro If $VDDIO_{micro}$ = 2.5V or 3.3V : Tie to GND.

9.16 No Connect Pins

Table 16. No Connect Pins

HSBGA Ball	Signal Name	Type	Description
B1, C1, C2, C6, C7 C15, D1, D2, E1, E2, E15, F1, G1, G2, H1, H2, J1, J2, K1, L1, L2, M1, M2, N1, N2, P1, R1, R2, T1, T2, U1, U2, V1	NC	NC	These pins are no connects. Do not connect these pins together or to ground. Leave these pins unconnected (floating).

9.17 Power Supply Pins

Table 17. Power Supply Pins

HSBGA Ball	HSBGA Supply Name	Type	Nominal Supply Voltage (V)	Description
Digital I/O Power Supply Pins				
R5, R6, R7, R9, R11, R12	$VDDIO_{MAC}$	P	3.3V, 2.5V, 1.5V	The I/O power supplies on the VSC8244 are separated on the chip itself to facilitate support for different VDDIO supply voltages. These VDDIO supplies can be run independently at the voltages specified in the previous column.
L15	$VDDIO_{micro}$	P	3.3V, 2.5V, 1.5V	
K15	$VDDIO_{ctl}$	P	3.3V, 2.5V	
Digital Core Power Supply Pins				
H4, J4, P4, R4, R14, R15, J15, H15	VDDDIG	P	1.2V	Power for internal digital logic.
Analog Power Pins				
D4, L4, G15, F15, D13, D12, D11, D10, D9, D6, D5, C8, R16	VDD33	P	3.3V	General 3.3v analog power
E4, F4, H3, J3, M3, N3, R3, D15, D14	VDD12	P	1.2V	General 1.2v analog power

Table 17. Power Supply Pins *(continued)*

HSBGA Ball	HSBGA Supply Name	Type	Nominal Supply Voltage (V)	Description
Ground Pins				
G[7:12], H[7:12], J[7:12], K[7:12], L[7:12], F2, P2, P3, G4, K4, K3, K2, L3, M4, N4, P15, N15, C14, C13, C12, C11, D8, D7	VSSS	G	0V	Ground for all blocks except parallel I/O
M[7:12], M15	VSSIO	G	0V	Ground for parallel I/O Note: For the 216-pin package this is integrated into the exposed pad.

9.18 Power Supply and Associated Functional Pins

Table 18. Power Supply and Associated Functional Pins

Power Supply Pins	Nominal Voltages	Associated Functional Pins
$VDDIO_{MAC}$	3.3V, 2.5V, 1.5V	TXD[3:0], TX_CTL, TX_CLK, RXD[3:0], RX_CTL, RX_CLK, TXREF_n, $CLK125_{MAC}$
$VDDIO_{micro}$	3.3V, 2.5V, 1.5V	$\overline{SOFT\_RESET}$, $\overline{RESET}$, MDINT_n, MDIO, MDC, MICROREF, $CLK125_{micro}$
$VDDIO_{ctl}$	3.3V, 2.5V	TDI, TDO, TMS, TCK, $\overline{TRST}$, EEDAT, EECLK
VDD33	3.3V	LED[4:0], CMODE[7:0], TXVN, TXVP, REF_REXT, REF_FILT, XTAL1

10 System Schematics

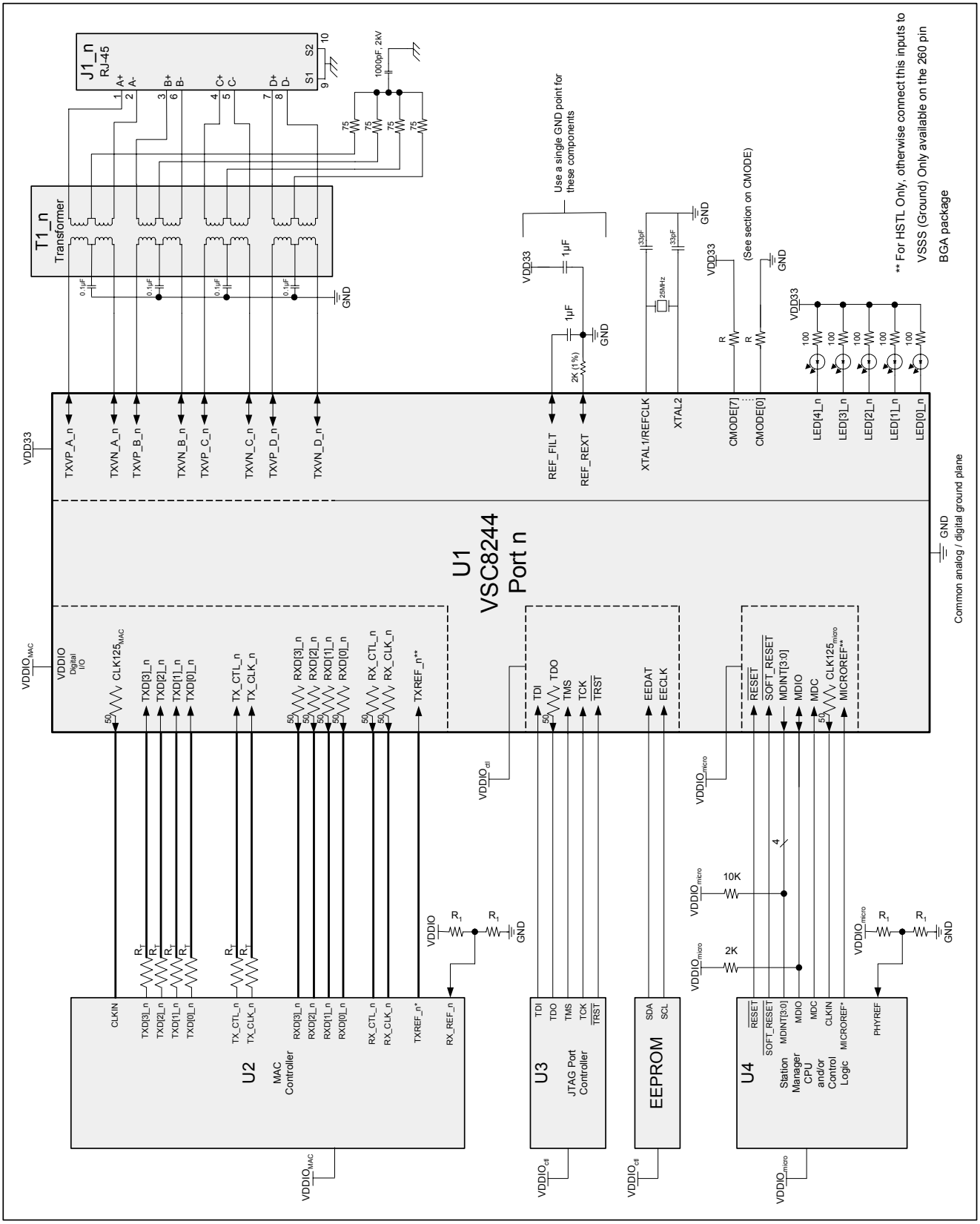


Figure 6. General System Schematic (shown with RGMII and 3.3V I/O)

10.1 Input Clock Options

The VSC8244 can be driven by three different clocking schemes providing the end user with design flexibility for clock strategy.

10.1.1 Crystal Clock Option

A 25MHz crystal can be connected to the XTAL1 and XTAL2 pins as described in Section 9.11: “System Clock Interface Pins”. The OSCEN will need to be pulled high and the PLLMODE can be left floating. Please refer to Figure 7

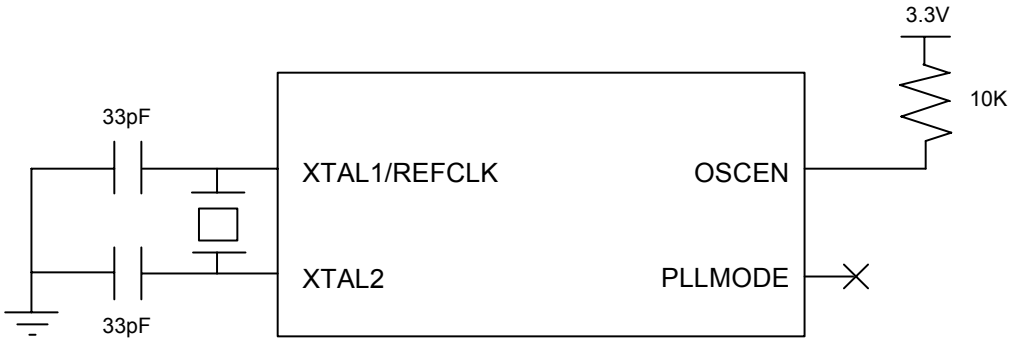


Figure 7. Crystal Clock Option

10.1.2 25MHz Reference Clock Option

A 25MHz reference clock can be connected to XTAL1, with XTAL2 left floating as described in Section 9.11: “System Clock Interface Pins”. The OSCEN and the PLLMODE can be left floating. Please refer to Figure 8.

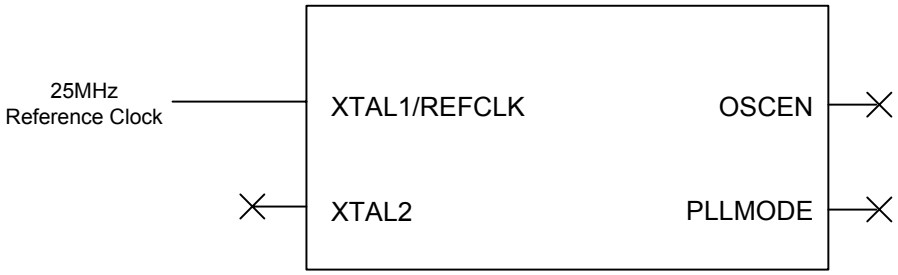


Figure 8. 25 MHz Reference Clock Option

10.1.3 125MHz Reference Clock Option

A 125MHz reference clock can be connected to XTAL1, with XTAL2 left floating as described in Section 9.11: “System Clock Interface Pins”. The OSCEN can be left floating and the PLLMODE will need to be pulled high. Please refer to Figure 9.

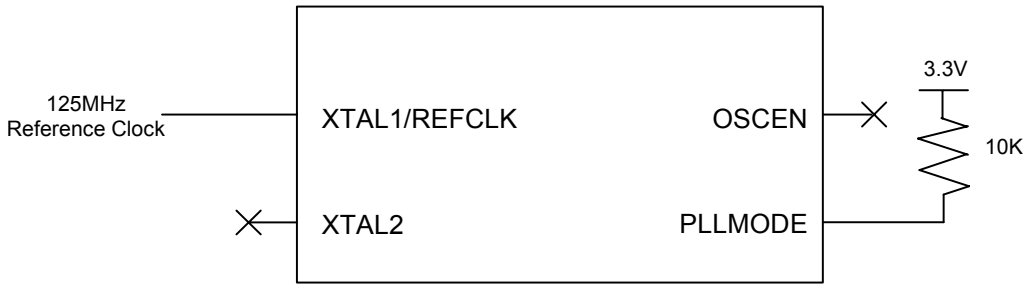


Figure 9. 125 MHz Reference Clock Option

10.2 Analog Bias Pins Configuration

For proper operation, the VSC8244 must generate an on-chip band gap reference voltage at the REF_FILT pin. For this, the following components are required for each VSC8244 in the system as specified in Section 9.14: "Analog Bias Pins".

- 2.00kΩ resistor, 1% tolerance.
- Two 1uF capacitors, with 10% tolerance or better.

The resistor will connect between the REF_REXT pin and ground. One 1uF capacitor will connect between the REF_FILT pin and ground. The other capacitor will connect between VDD33 voltage supply and ground.

For best performance, special consideration for the ground connection of the voltage reference circuit is necessary to prevent bus drops which would cause inaccuracy in the reference voltage. Each of these ground connections should join together at a small common area and then a short trace should then connect this area to the main ground plane (Refer to Figure 10). All of these components should be placed as close as possible to the VSC8244.

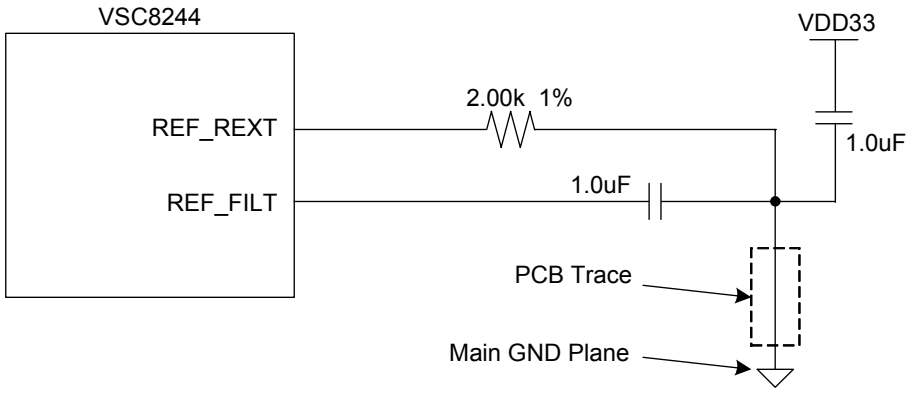


Figure 10. Analog Bias Pins Ground Connection Diagram

11 MAC Interfaces

11.1 RGMII MAC I/F

RGMII MAC I/F mode clocks data at 125MHz in 1000BT mode, 25MHz in 100BT mode, or 2.5MHz in 10BT mode. The I/O power supply can be 3.3V, 2.5V, or 1.5V HSTL-compliant.

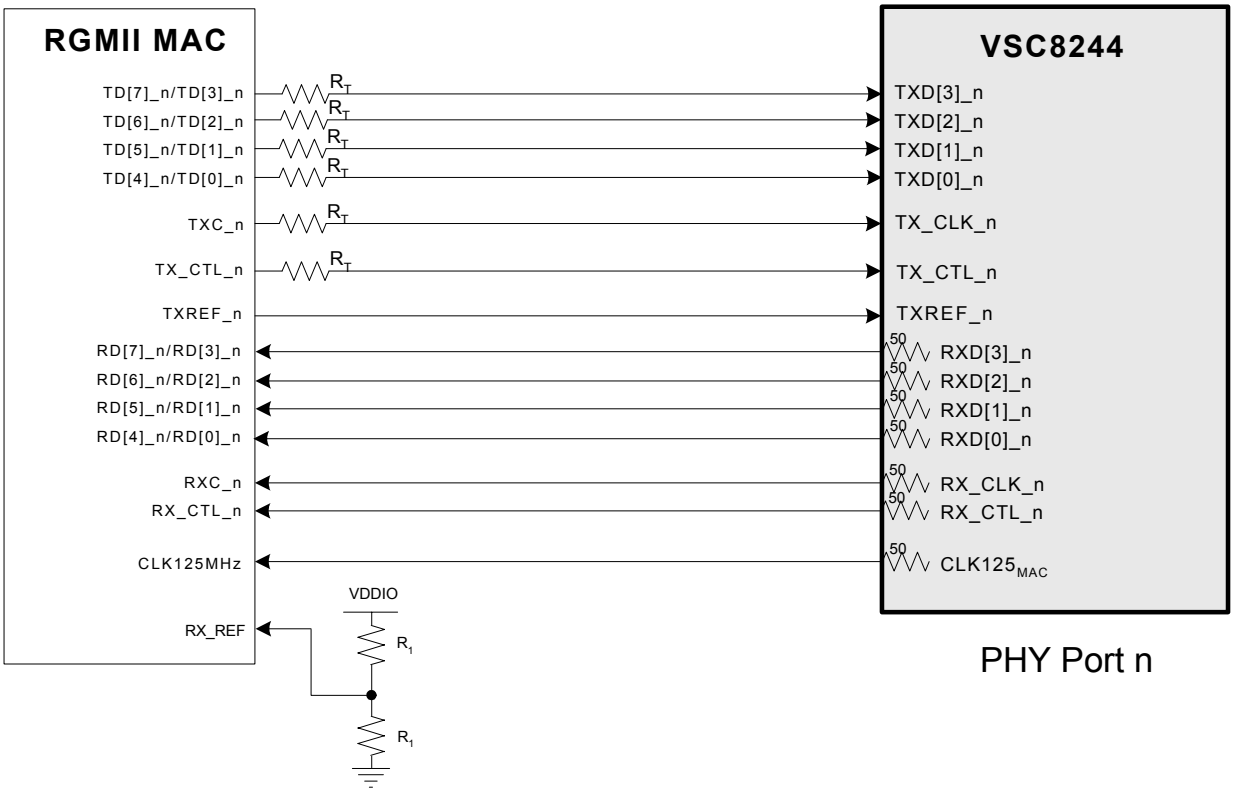


Figure 11. RGMII MAC Interface

Note:

- MAC TX lines are usually series- terminated close to the source (at the MAC), with R_T typically ~22Ω.
- Since the VSC8244 includes on-chip, calibrated, series termination resistors, no external series termination resistors are required on the PCB.
- All PCB traces should be 50Ω controlled impedance traces.
- The VSC8244 includes innovative on-chip timing compensation circuitry to simplify PCB design and layout. Please refer to Section 25.8.1: "RGMII Mode Timing" for more information.
- RX_REF should be set to VDDIO/2 through an external resistor divider network (HSTL 1.5V I/O only).
- TXREF_n is only available in the 260-pin HSBGA package
- TXREF_n should be tied to ground if VDDIO = 3.3V or 2.5V.
- TXREF_n should be connected to the MAC's HSTL reference when VDDIO = 1.5V HSTL.

11.2 RTBI MAC I/F

RTBI MAC I/F mode, selected by setting the MAC I/F selection bits to RTBI mode Register 23.15:12, clocks data at 125MHz.

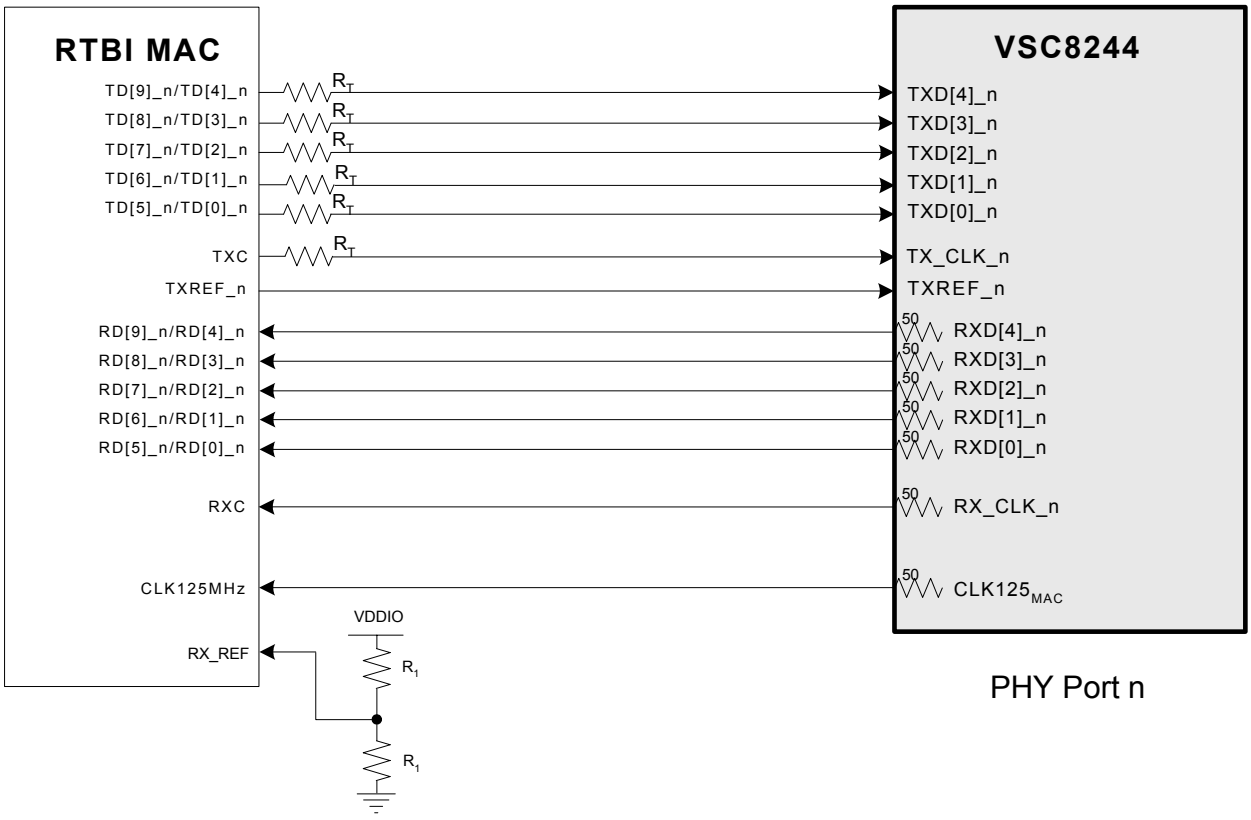


Figure 12. RTBI MAC Interface

Note:

- MAC TX lines are usually terminated on the source side (at the MAC), with R_T typically ~22Ω.
- Since the VSC8244 includes on-chip, calibrated, series termination resistors, no external series termination resistors are required on the PCB.
- All PCB traces should be 50Ω controlled impedance traces.
- The VSC8244 includes innovative on-chip timing compensation circuitry to simplify PCB design and layout. Please refer to Section 25.8.2: "RTBI Mode Timing" for more information.
- RX_REF should be set to VDDIO/2 through an external resistor divider network (HSTL 1.5V I/O only).
- TXREF_n is only available in the 260-pin HSBGA package
- TXREF_n should be tied to ground if VDDIO = 3.3V or 2.5V.
- TXREF_n should be connected to the MAC's HSTL reference when VDDIO = 1.5V HSTL.

12 Twisted Pair Interface

The twisted pair interface on the VSC8244 is fully compliant with the IEEE802.3-2000 specification for CAT-5 media. The VSC8244 PHY, unlike other traditional Gigabit PHYs, has all passive components (required to connect the PHY's CAT-5 interface to an external 1:1 transformer) fully integrated into the device. The connection of the twisted pair interface is shown in Figure 13:

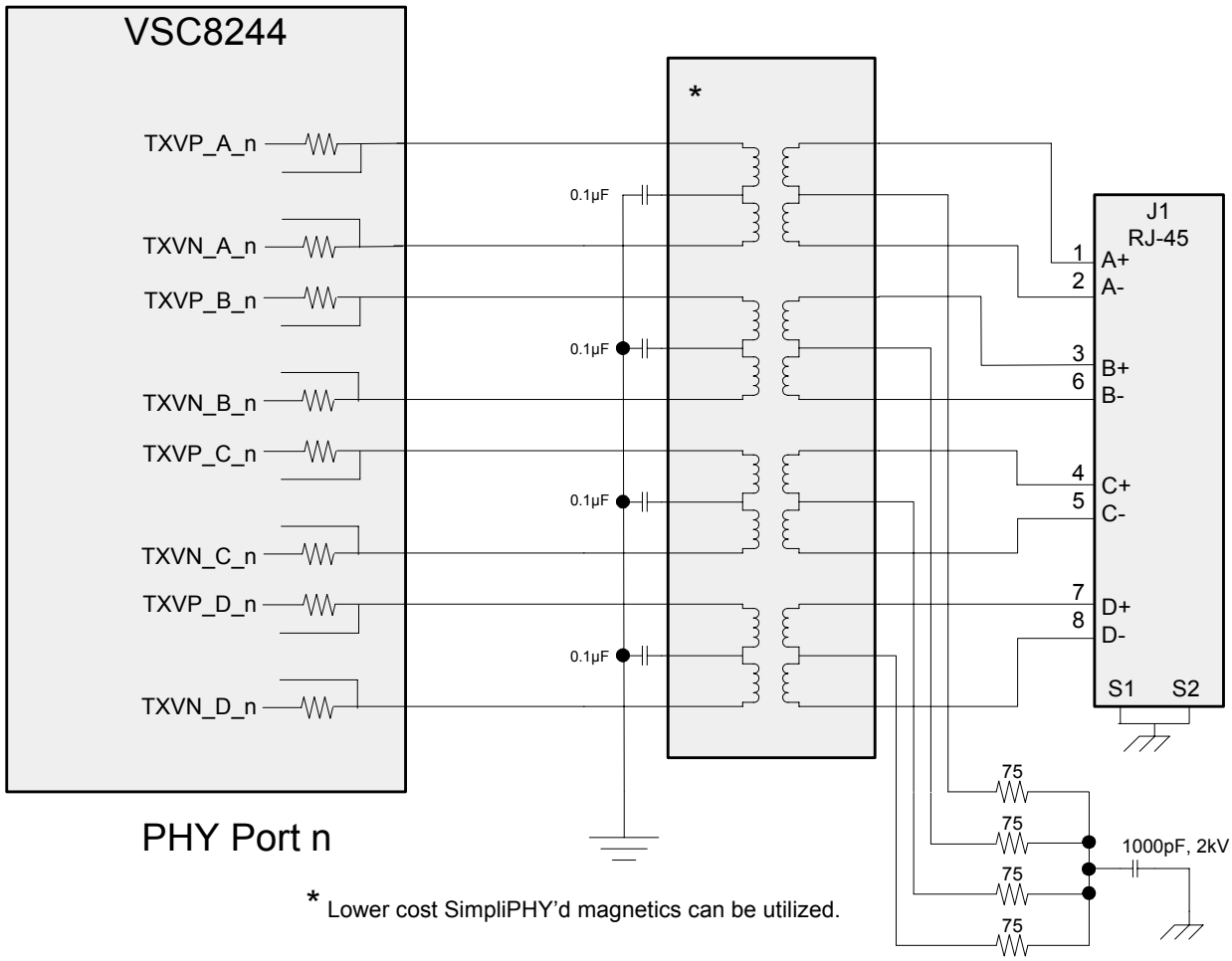


Figure 13. Twisted Pair Interface

12.1 Twisted Pair Autonegotiation (IEEE802.3 Clause 28)

The VSC8244 supports twisted pair autonegotiation, as defined in IEEE 802.3-2002 clause 28. This process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, autonegotiation can determine speed, duplex, and MASTER/SLAVE modes for 1000BASE-T. Autonegotiation also allows the local MAC to communicate with the Link Partner MAC (via optional "Next-Pages") to set attributes that may not be defined in the standard. If the link partner does not support autonegotiation, the VSC8244 will automatically use parallel-detect to select the appropriate link speed.

Clause 28 twisted-pair autonegotiation can be disabled by clearing MII Register bit 0.12. If autonegotiation is disabled, the operating speed and duplex mode of the VSC8244 is determined by the state of MII Register bits 0.6, 0.13 and MII Register bit 0.8.

12.2 Twisted Pair Auto MDI/MDI-X Function

For trouble-free configuration and management of Ethernet links, the VSC8244 includes robust Automatic Crossover Detection functionality for all three speeds on the twisted pair interface (10BASE-T, 100BASE-TX, and 1000BASE-T) – fully compliant with the IEEE standard. In addition, the VSC8244 detects and corrects polarity errors on all MDI pairs, which is not required by the standard. Both the Automatic MDI/MDI-X and Polarity Correction functions are enabled by default. However, complete user control of these two features is contained in MII Register bit 18.5 and MII Register bit 18.4. Status bits for each of these functions are indicated in MII Register 28.

The VSC8244's Automatic MDI/MDI-X algorithm will successfully detect, correct, and operate with any of the MDI wiring pair combinations listed in the following table:

Table 19. Accepted MDI Pair Connection Combinations

	RJ-45 Connections				Comments
	1,2	3,6	4,5	7,8	
MDI Pair Connection Combinations Accepted by VSC8244	A	B	C	D	Normal MDI mode
	B	A	D	C	Normal MDI-X mode
	A	B	D	C	MDI mode Pair swap on C and D pairs
	B	A	C	D	MDI-X mode Pair swap on C and D pairs

12.3 Auto MDI/MDI-X in Forced 10/100 Link Speeds

The VSC8244 includes the ability to perform Auto MDI/MDI-X even when auto-negotiation is disabled (MII Register 0.12 = 0) and the link is forced into 10/100 link speeds. In order to enable this feature, additional MII register write settings are also needed in the following order:

To enable Auto MDI/MDI-X in forced 10/100 link speeds:

- Write MII Register 31 = 0x52b5
- Write MII Register 18 = 0x0012
- Write MII Register 17 = 0x2803
- Write MII Register 16 = 0x87fa
- Write MII Register 31 = 0x0000

To disable Auto MDI/MDI-X in forced 10/100 link speeds:

- Write MII Register 31 = 0x52b5
- Write MII Register 18 = 0x0012
- Write MII Register 17 = 0x3003
- Write MII Register 16 = 0x87fa
- Write MII Register 31 = 0x0000

12.4 Twisted Pair Link Speed Downshift

In addition to automatic crossover detection, the VSC8244 supports an automatic link speed "downshift" option for operation in cabling environments incompatible with 1000BASE-T. When this feature is enabled, the VSC8244 will automatically change its 1000BASE-T autonegotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T. This is especially useful in setting up networks using older cable installations which may include only pairs A and B and not pairs C and D. The link speed downshift feature is configured and monitored through MII Register bits 20E.4:1.

13 Transformerless Ethernet Operation for PICMG 2.16 and 3.0 IP-based Backplanes

The twisted pair interface supports 10/100/1000BT Ethernet for backplane applications such as those specified by the PICMG 2.16 and 3.0 specifications for 8-pin channels. With proper AC coupling, the typical category-5 transformer (magnetics) can be removed and replaced with capacitors. For more information, refer to Application Note: Transformerless Ethernet Concept and Applications.

By enabling the PICMG reduced power mode (MII Register bit 24.12 = 1), power consumption can be reduced to under 600mW/port. For specific backplane applications it is possible for further reductions in power consumption (<500 mW/port). To configure the device for this mode, the following MII register write settings are also needed in the following order:

- Write MII Register 31 = 0x2a30
- Write MII Register 22 = 0x4900
- Write MII Register 31 = 0x0000

14 Serial Management Interface (SMI)

The VSC8244 includes a Serial Management Interface, or “SMI”, that is fully compliant with the IEEE 802.3-2000 specifications. The SMI interface provides access to various status and control registers within the VSC8244. This MII Register set is comprised of a block of thirty-two 16-bit registers, which are segmented into two pages: PAGE0 (main page) and PAGE1 (extended page). The desired register page is selected by setting the page number in Register 31. Registers 0 through 10, in addition to Register 15, (all main page) are required for IEEE compliance. The VSC8244 implements all IEEE-required registers, in addition to several others, providing additional performance-monitoring capabilities. See Section 24: "MII Register Descriptions" for more information.

The SMI is a two pin, synchronous serial interface, with bidirectional data on MDIO being clocked on the rising edge of MDC. The SMI can be clocked at a rate from 0 to 12.5MHz, depending on the total load on MDIO. An external pull-up is required on MDIO; it is typically 2kΩ, but depends on the total load on MDIO.

Data is transferred over the SMI using 32-bit frames with an optional and arbitrary length preamble. The SMI frame format is described in the following table.

Table 20. SMI Frame Format

	Direction from VSC8244	Preamble	Start of Frame	Op Code	PHY Address	Register Address	Turn-Around	Data	Idle
# of bits		1+	2	2	5	5	2	16	?
Read	Output	Z’s	ZZ	ZZ	Z’s	Z’s	Z0	data	Z’s
	Input	1’s	01	10	addr	addr	ZZ	Z’s	Z’s
Write	Output	Z’s	ZZ	ZZ	Z’s	Z’s	ZZ	Z’s	Z’s
	Input	1’s	01	01	addr	addr	10	data	Z’s

- Idle: During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical “1” state. Since idle mode should not contain any transitions on MDIO, the number of bits is undefined during idle.
- Preamble: For the VSC8244, the preamble is optional. By default, preambles are not expected or required. The preamble is a string of “1”s. If it exists, the preamble must be at least one bit, but otherwise may be arbitrarily long. See MII Register 1.6 for more information.
- Start of frame: A “01” pattern indicates the start of frame. If these bits are anything other than “01”, all following bits are ignored until the next “preamble:0” pattern is detected.

- Operation code: A “10” pattern indicates a read. A “01” pattern indicates a write. If these bits are anything other than “01” or “10”, all following bits are ignored until the next “preamble” pattern is detected.
- PHY address: The next five bits are the PHY address. The VSC8244 responds to a message frame only when the received PHY address matches its physical address. Its physical address has 5 bits, 4:0. Bits 4:2 is set by the CMODE pin configuration setting. Bits 1:0 represent which PHY within the device is being addressed.
- Register address: The next five bits are the register address.
- Turn-around: The next two bits are “turn-around” (TA) bits. They are used to avoid contention when a read operation is performed on the MDIO. During read operations, the VSC8244 will drive the second TA bit, which is a logical “0”.
- Data: The next sixteen bits are data bits. When data is being read from the PHY, data is valid at the output of the PHY from one rising edge of MDC to the next rising edge of MDC. When data is being written to the PHY, data must be valid around the rising edge of MDC.
- Idle: The sequence is repeated.

The following two figures diagram SMI read and SMI write operations.

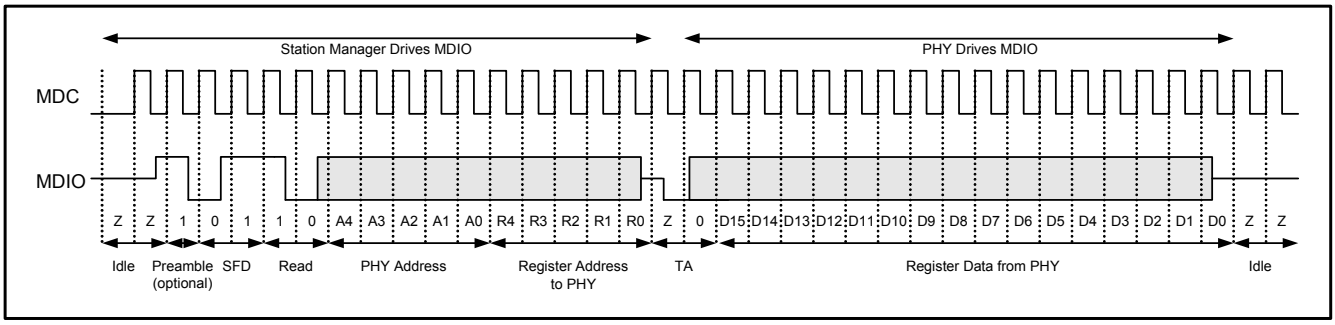


Figure 14. MDIO Read Frame

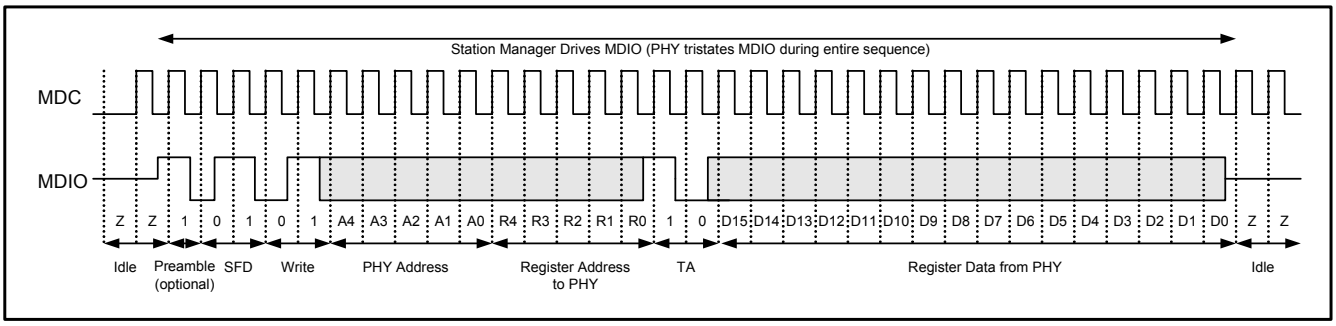


Figure 15. MDIO Write Frame

14.1 SMI Interrupt

The SMI includes an output signal MDINT_n for signalling the Station Manager when certain events occur in the PHY. A separate MDINT_n pin in included for each PHY in the VSC8244. Each MDINT_n pin can be configured for open-drain (active-low), or open-source (active-high) by tying the pin to either a pull-up resistor to $VDDIO_{micro}$ (see Figure 16), or to a pull-down resistor to GND (see Figure 17). If only one interrupt pin is required, each MDINT_n pin can be tied together to a single pull-up or pull-down resistor in a wired-OR configuration.

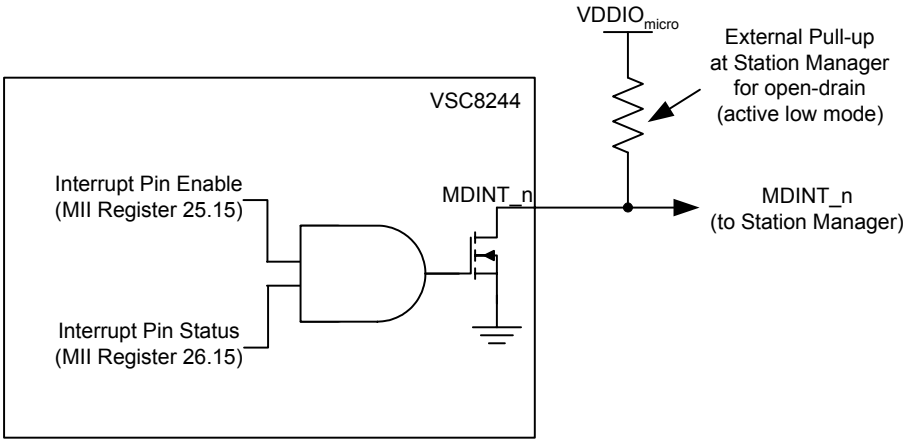


Figure 16. Logical Representation of Open-Drain (Active-Low) MDINT_n Pin

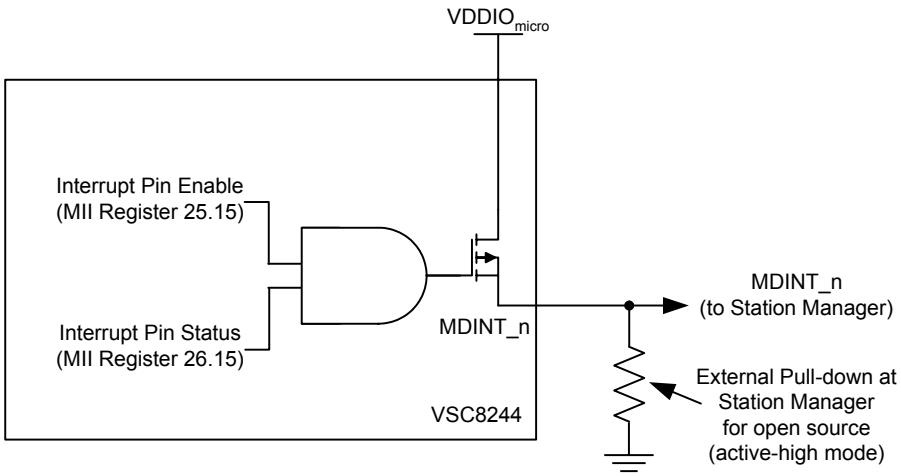


Figure 17. Logical Representation of Open-Source (Active-High) MDINT_n Pin

When the VSC8244 PHY generates an interrupt, the MDINT_n pin is asserted (driven either high or low, depending on the external resistor connection) if the interrupt pin enable bit (MII Register 25.15) is set.

15 Parallel LED Interface

The VSC8244 contains dedicated pins to drive 5 LEDs directly for each PHY port.

For power savings, all LED outputs can be configured to pulse at 5kHz with a 20% duty cycle by setting LED pulsing enable (MII Register 27.4 = 1). All LED outputs are active-low, and driven with 3.3V from the VDD33 power supply.

Table 21. LED Function Assignments

LED Configuration Bits	MII Register Bit	Value	LED Function Selection
LED Pin 4 Config [1:0]	27.15:14	11	Link/Activity
		10	Fault
		01	Activity
		00	Duplex/Collision
LED Pin 3 Config [1:0]	27.13:12	11	RX
		10	Reserved
		01	Duplex/Collision
		00	Collision
LED Pin 2 Config [1:0]	27.11:10	11	TX
		10	Link/Activity
		01	Duplex/Collision
		00	Link10/Activity
LED Pin 1 Config [1:0]	27.9:8	11	Link100/1000/Activity
		10	Link/Activity
		01	Link10/100/Activity
		00	Link100/Activity
LED Pin 0 Config [1:0]	27.7:6	11	RX
		10	Fault
		01	Link/Act (with serial output on LED pins 1 and 2)
		00	Link1000/Activity

For flexibility, 14 LED output functions can be selected for each PHY port. These functions are summarized in the following table:

Table 22. LED Functions

Function Name	LED State	Description
Link1000/Activity	1	No link in 1000BASE-T
	0	Valid 1000BASE-T link
	Pulse-stretch/Blink[1,2]	(optional) Valid 1000BASE-T link and activity present
Link100/Activity	1	No link in 100BASE-Tx
	0	Valid 100BASE-Tx link
	Pulse-stretch/Blink[1,2]	(optional) Valid 100BASE-Tx link and activity present

Table 22. LED Functions *(continued)*

Function Name	LED State	Description
Link10/Activity	1	No link in 10BASE-T
	0	Valid 10BASE-T link
	Pulse-stretch/Blink[1,2]	(optional) Valid 10BASE-T link and activity present
Link10/100/Activity	1	No link in 10BASE-T or 100BASE-Tx
	0	Valid 10BASE-T link or valid 100BASE-Tx link
	Pulse-stretch/Blink[1,2]	(optional) Valid 10BASE-T link or valid 100BASE-Tx link and activity present
Link100/1000/Activity	1	No link in 100BASE-Tx or 1000BASE-T
	0	Valid 100BASE-Tx link or valid 1000BASE-T link
	Pulse-stretch/Blink[1,2]	(optional) Valid 100BASE-Tx link or valid 1000BASE-T link and activity present
Link/Activity	1	No link in any speed
	0	Valid link in any speed
	Pulse-stretch/Blink[1,2]	Valid link in any speed and activity present
Collision	1	No collision detected
	Pulse-stretch/blink[2]	Collision detected
Activity	1	No activity
	Pulse-stretch/blink[2]	Activity present
Fault	1	No IEEE Clause 28 autonegotiation fault
	0	IEEE Clause 28 autonegotiation fault
Serial	**	See Section 16: "Serial LED Output"
Duplex/Collision	1	Link established in half-duplex mode, or no link established
	0	Link established in full-duplex mode
	Pulse-stretch/Blink[2,3]	(optional) Link established in half duplex mode and collisions present
Rx	1	No activity on Rx side
	Pulse-stretch/blink[2]	Activity present on Rx side
Tx	1	No activity on Tx side
	Pulse-stretch/blink[2]	Activity present on Tx side

[1] Link functions can be combined with Activity function using an option bit below.
[2] Function can either blink or be pulse-stretched when active. This behavior is selected using an option bit below.
[3] Duplex function can be combined with Collision function using an option bit below.

In addition to function selection, several option bits (found in MII Register 27) are available for the LED outputs. These are summarized below:

Table 23. LED Output Options

LED Option Bits	MII Register Bit	Value	LED Function Selection
LED Blink/Pulse-Stretch Rate	27.5	1	10Hz blink rate/ 100ms pulse-stretch
		0	5Hz blink rate/ 200ms pulse-stretch
LED Pulsing Enable	27.4	1	When active, LED outputs will be pulsed at 5KHz, 20% duty cycle for power savings
		0	When active, LED outputs will remain at a static low
LED Pulse-Stretch/Blink Select	27.3	1	Collision, Activity, Rx and Tx LED outputs will be pulse-stretched when active
		0	Collision, Activity, Rx and Tx LED outputs will blink when active
LED combine Link Status with Activity	27.2	1	Link LEDs indicate link status only
		0	Link LEDs will blink or flash when activity is present. Blink/flash behavior is selected by Pulse-Stretch Enable bit.
LED combine Link10/100/1000 with Activity	27.1	1	Link10, Link100, Link1000, Link10/100, Link 100/1000 LEDs indicate link status only
		0	Link10, Link100, Link1000, Link10/100, Link 100/1000 LEDs will blink or flash when activity is present. Blink/flash behavior is selected by Pulse-Stretch Enable bit.
LED combine Collision with Duplex Status	27.0	1	Duplex LED indicates duplex status only
		0	Duplex LED will blink or flash when collision is present. Blink/flash behavior is selected by Pulse-Stretch Enable bit.

16 Serial LED Output

A serial output option is available which allows access to all LED signals through two pins. This option is selected by setting LED Pin 0 configuration bits to 01 on PHY0. In this mode, LED[1]_0 acts as the serial data pin and LED[2]_0 acts as the serial clock pin. These two pins will then output LED status for all 4 PHYs. The serial mode will clock out the 44 LED status bits on the rising edge of the serial clock.

The serial bitstream outputs each LED signal as as shown in the table below, beginning with PHY0 and ending with PHY3. The behavior of each LED signal is described in Table 22 on page 38. The individual signals shall be clocked out in the following order:

Table 24. Serial LED Output Data

PHY0	PHY1	PHY2	PHY3
1. Link1000/Activity	12. Link1000/Activity	23. Link1000/Activity	34. Link1000/Activity
2. Link/Activity	13. Link/Activity	24. Link/Activity	35. Link/Activity
3. Link100/Activity	14. Link100/Activity	25. Link100/Activity	36. Link100/Activity
4. Activity	15. Activity	26. Activity	37. Activity
5. Link10/Activity	16. Link10/Activity	27. Link10/Activity	38. Link10/Activity
6. Duplex/Collision	17. Duplex/Collision	28. Duplex/Collision	39. Duplex/Collision
7. Tx	18. Tx	29. Tx	40. Tx
8. Collision	19. Collision	30. Collision	41. Collision
9. Rx	20. Rx	31. Rx	42. Rx
10. Fault	21. Fault	32. Fault	43. Fault
11. Reserved	22. Reserved	33. Reserved	44. Reserved

17 Test Mode Interface (JTAG)

The VSC8244 supports the Test Access Port and Boundary Scan Architecture IEEE 1149.1 standards. The device includes an IEEE 1149.1 conformant test interface, often referred to as a “JTAG TAP Interface”. IEEE 1149.1 defines test logic to provide standardized test methodologies for:

- Testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate
- Testing the integrated circuit itself during IC and systems manufacture
- Observing or modifying circuit activity during the component’s normal operation

The JTAG Test interface logic on the VSC8244, accessed through a Test Access Port (TAP) interface, consists of a boundary-scan register and other logic control blocks. The TAP controller includes all IEEE-required signals (TMS, TCK, TDI, and TDO), in addition to the optional asynchronous reset signal $\overline{\text{TRST}}$. Refer to JTAG TAP Signal Descriptions section for additional information about these pins.

The following figure diagrams the TAP and Boundary Scan Architecture.

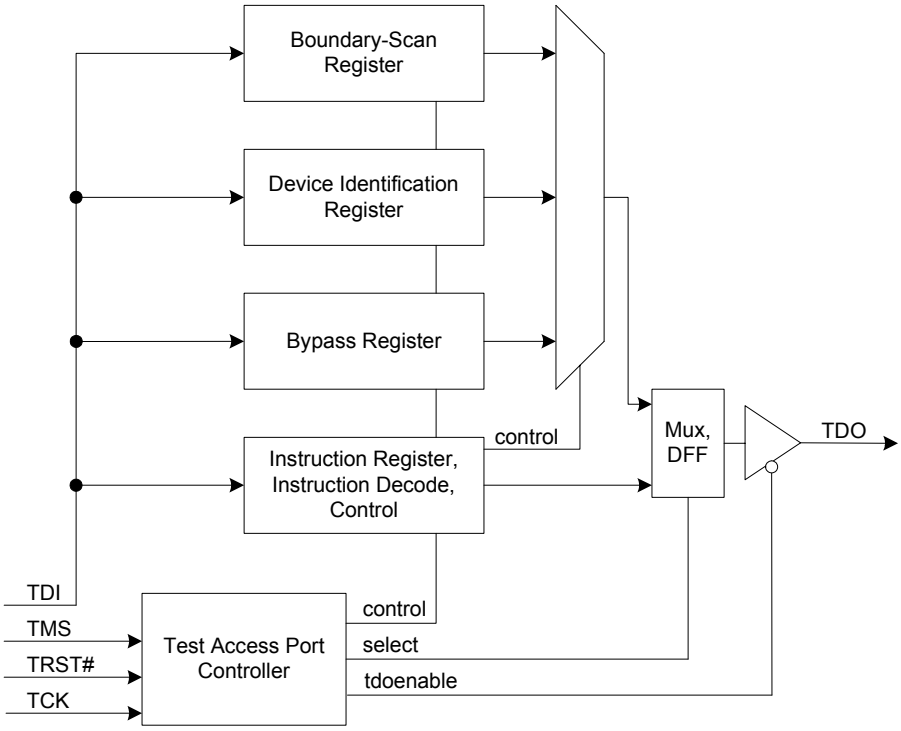


Figure 18. Test Access Port and Boundary Scan Architecture

The VSC8244 also includes the optional Device Identification Register, shown in the following table, which allows the manufacturer, part number, and version number of the device to be determined through the TAP Controller.

See Chapter 11 of the IEEE 1149.1-1990 specifications for more details. Also, note that some of the information in the identification register is duplicated in the IEEE-specified bit fields in MII Register 3 (PHY Identifier Register #2).

Table 25. JTAG Device Identification Register Description

Description	Device Version Number (or Revision Code)	Part Number (or Model Number)	Vitesse's Manufacturer Identity	LSB
Bit Field	31 - 28	27 - 12	11 - 1	0
Binary Value	Silicon Revision C = 0010	1000 0010 0100 0100	001 1001 1000	1

17.1 Supported Instructions and Instruction Codes

After a TAP reset, the Device Identification Register is serially connected between TDI and TDO by default. The TAP Instruction Register is loaded either from a shift register (when a new instruction is shifted in), or, if there is no new instruction in the shift register, a hard-wired default value of 0110 (IDCODE) is loaded. Using this method, there is always a valid code in the instruction register, and the problem of toggling instruction bits during a shift is avoided. Unused codes are mapped to the BYPASS instruction.

The VSC8244 supports the instruction codes listed in the following and described below.

Table 26. JTAG Interface Instruction Codes

Instruction	Code	Selected Register	Register Width	Specification
EXTEST	0000	Boundary-Scan Register	196	Mandatory IEEE 1149.1
SAMPLE/PRELOAD	0001	Boundary-Scan Register	196	Mandatory IEEE 1149.1
IDCODE	0110	Device Identification Register	32	Optional IEEE 1149.1
CLAMP	0010	Bypass Register	1	Optional IEEE 1149.1
HIGHZ	0011	Bypass Register	1	Optional IEEE 1149.1
BYPASS	0111	Bypass Register	1	Mandatory IEEE 1149.1
NANDTEST	0101	Bypass Register	1	Optional IEEE 1149.1
Reserved	0100, 1000 - 1111			

EXTEST
The mandatory EXTEST instruction allows testing of off-chip circuitry and board-level interconnections by sampling input pins and loading data onto output pins. Outputs are driven by the contents of the boundary-scan cells, which have to be updated with valid values (with the PRELOAD instruction) prior to the EXTEST instruction.

SAMPLE/PRELOAD
The mandatory SAMPLE/PRELOAD instruction allows a snapshot of inputs and outputs during normal system operation to be taken and examined. It also allows data values to be loaded into the boundary-scan cells prior to the selection of other boundary-scan test instructions.

IDCODE
The optional IDCODE instruction provides the version number (bits 31:28), part number (bits 27:12), and Vitesse's manufacturer identity (bits 11:1) to be serially read from the VSC8244. See Table 25: "JTAG Device Identification Register Description" for the VSC8244-specific values for this instruction.

CLAMP
The optional CLAMP instruction allows the state of the signals driven from the component pins to be determined from the

Boundary-Scan Register while the Bypass Register is selected as the serial path between TDI and TDO. While the CLAMP instruction is selected, the signals driven from the component pins will not change.[1]

HIGHZ
The optional HIGHZ instruction places the component in a state in which *all* of its system logic outputs are placed in a high impedance state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring a risk of damage to the component. This makes it possible to use a board where not all of the components are compatible with the IEEE 1149.1 standard.[1]

BYPASS
The Bypass Register contains a single shift-register stage and is used to provide a minimum-length serial path (one TCK clock period) between TDI and TDO to bypass the device when no test operation is required.

NANDTEST
NANDTEST is an internal command used to activate the NAND Tree test mode.

17.2 Boundary-Scan Register Cell Order

All inputs and outputs are observed in the Boundary-Scan Register cells. All outputs are additionally driven by the contents of Boundary-Scan Register cells. Bidirectional pins have all three related Boundary-Scan Register cells: the input, the output, and the control. The full boundary scan cell order is available as a .BSD file format.

[1]Following the use of this instruction, the on-chip system logic may be in an indeterminate state that will persist until a system reset is applied. Therefore, the on-chip system logic must be reset on return to normal (i.e., non-test) operation.

18 VeriPHY Cable Diagnostics

The VSC8244 provides a comprehensive suite of cable diagnostic functions that are available through SMI reads and writes. Vitesse provides a library of routines that enable a variety of cable operating conditions and status to be accessed. These functions have the ability to identify the cable length and operating conditions, and to isolate a variety of common faults that can occur on the CAT-5 twisted pair cabling. Contact Vitesse Semiconductor for access to the VeriPHY® library of routines.

The following functions are available:

- Coupling between cable pairs
- Cable pair termination
- Cable Length
- Using VeriPHY® in normal operating mode

18.1 Coupling Between Cable Pairs

Anomalous coupling between cable pairs can be caused by shorted wires, improper termination, or high crosstalk resulting from an incorrect wire map. These conditions can all prevent the VSC8244 from establishing a link in any speed.

18.2 Cable Pair Termination

Proper termination of CAT-5 cable requires a 100-ohm differential impedance between the positive and negative cable terminals. IEEE802.3 allows for a termination of as high as 115-ohms or as low as 85-ohms. If the termination falls outside of this range, it will be reported as an anomalous termination by the VeriPHY® cable diagnostics. The diagnostics can also determine the presence of an open or shorted cable pair.

18.3 Cable Length

When properly terminated, VeriPHY reports the approximate cable length in meters for each of the four cable pairs A, B, C, and D.

18.4 Using VeriPHY in normal operating mode

If a link is established on the twisted pair interface in 1000BASE-T mode, the VeriPHY® cable diagnostics can run without disruption of the link or of any data transfer. However, if a link is established in 100BASE-TX or 10BASE-T, the VeriPHY® cable diagnostics will cause the link to drop while the diagnostics are running. Once the diagnostics are finished, the link will be reestablished.

19 ActiPHY Power Management

In addition to the IEEE-specified power-down control bit (MII Register 0.11), the VSC8244 implements an ActiPHY™ power management mode. This mode enables support for power-sensitive applications such as laptop computers with Wake-on-LAN™ capability. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power-down the PHY. The PHY 'wakes up' at a programmable interval and attempts to 'wake-up' the link partner PHY by sending either a fast link pulse (FLP) over copper media.

The ActiPHY™ power management mode can be set at any time on a per port basis during normal operation by setting MII Register 28.6 = 1. When ActiPHY™ is enabled and the PHY is in the "Low Power" or "LP Wake-up" states, by default a 25MHz clock signal is sent out on the RX_CLK pin. This function can be disabled by setting MII Register Bit 23.5 = 0.

19.1 Operation in ActiPHY Mode

There are three PHY operating states when Enhanced ActiPHY™ mode is enabled:

- Low power state
- LP Wake up state
- Normal operating state (link up state)

The PHY switches between the low power state and LP wake up state at a programmable rate (sleep timer) until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. When the PHY is in the normal operating state and link is lost, the PHY returns to the low power state after the link status time-out timer has expired. After reset, the PHY enters the low power state.

When autonegotiation is enabled in the PHY, the ActiPHY™ state machine will operate as described above. If autonegotiation is disabled and the link forced to 10BT or 100BTX modes while the PHY is in the low power state, the PHY continues to transition between the low power and LP Wake up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. If autonegotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

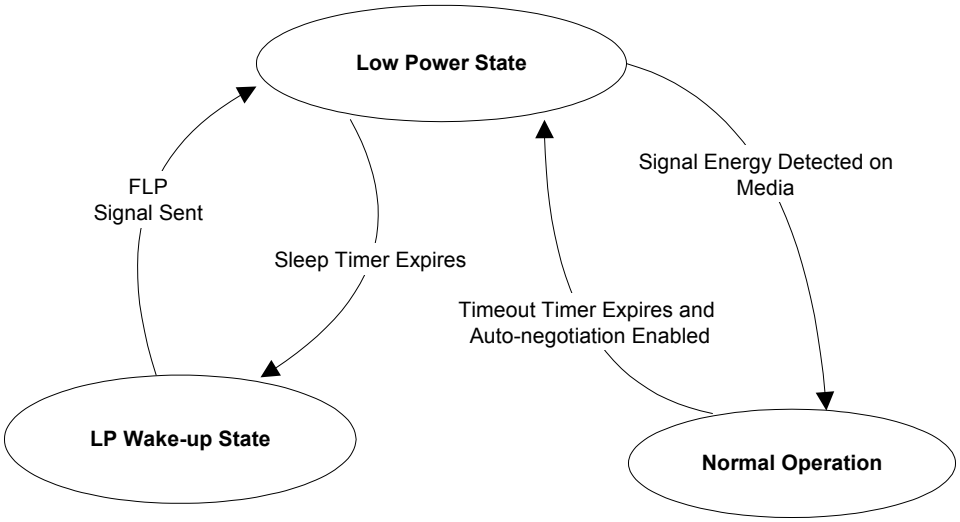


Figure 19. ActiPHY State Diagram

19.2 Low power state

In the low power state, all major digital blocks are powered down. However the following functionality is provided:

- SMI interface (MDC, MDIO, $\overline{\text{MDINT}}$_n)
- $CLK125_{MAC}$ and $CLK125_{MICRO}$

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low power state and transitions to the Normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Auto-negotiation capable link partner
- Auto-negotiation incapable (blind/forced) 100BTX only link partner
- Auto-negotiation incapable (blind/forced) 10BT only link partner
- Another PHY in Enhanced ActiPHY LP Wake Up state

In the absence of signal energy on the media pins, the PHY will transition from the low power state to the LP Wake up state periodically based on the programmable sleep timer. Two register bits (MII Register Bits 28.1:0) are provided to program the value of the sleep timer. The sleep timer can be programmed to 00 (1second), 01 (2 seconds), 10 (3 seconds) or 11 (4 seconds). The default value is 2 seconds. The actual sleep time duration is randomized by -80ms to +60ms to avoid two linked PHYs in ActiPHY^{TM} mode from entering a lock-up state.

19.3 LP Wake up state

In this state, the PHY attempts to wake up the link partner. One complete FLP (Fast Link Pulse) is sent on both pairs A and B of the CAT5 media.

In this state the following functionality is provided-

- SMI interface (MDC, MDIO, $\overline{\text{MDINT}}$_n)
- $CLK125_{MAC}$ and $CLK125_{MICRO}$

After sending signal energy on the relevant media, the PHY returns to the Low power state.

19.4 Normal operating state

In this state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration programmed through a link status time-out timer and then enters the low power state. The Link Status Time-out timer can be programmed to 00 (1second), 01 (2 seconds), 10 (3 seconds) or 11 (4 seconds). The default value for this timer is 2 seconds.

20 Ethernet In-line Powered Device Support

20.1 Cisco In-Line Powered Device Detection

This feature is used for detecting in-line powered devices in Ethernet network applications. The VSC8244's in-line powered device detection mode can be part of a system that allows for IP-phone and other devices such as wireless access points to receive power from an Ethernet cable, similar to office digital phones receiving power from a PBX (Private Branch Exchange) office switch via the phone cable. This can eliminate the need for an IP-Phone to have an external power supply since the Ethernet cable provides power. It also enables the in-line powered device to remain active during a power outage (assuming the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, etc). Each of the 4 PHYs can independently perform in-line power detection. This mode is disabled by default and must be enabled for each PHY in order to perform in-line powered device detection. Please refer to additional information at http://www.cisco.com/en/US/products/hw/phones/ps379/products_tech_note09186a00801189b5.shtml.

20.2 In-Line Power Ethernet Switch Diagram

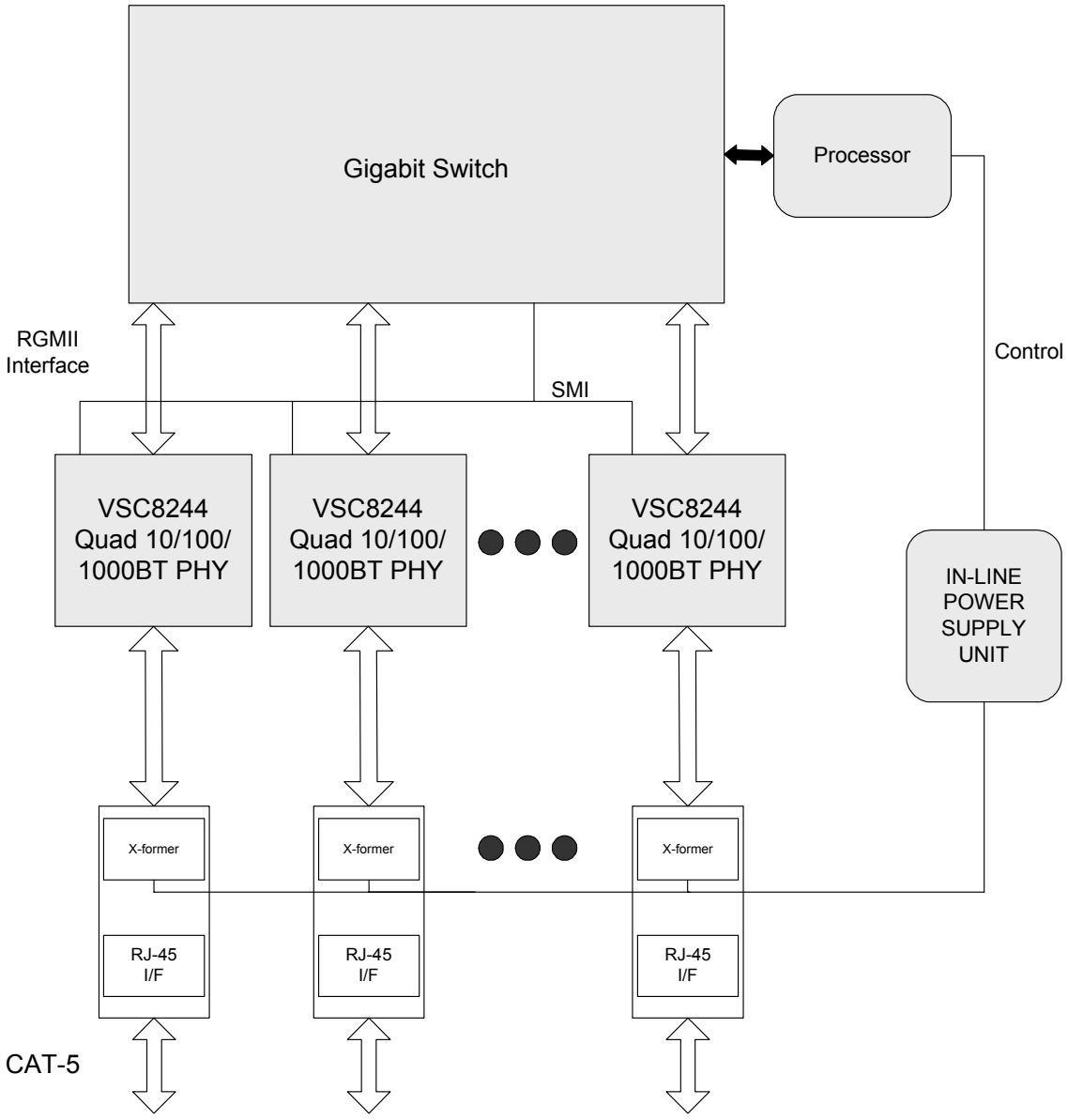


Figure 20. In-line Powered Ethernet Switch Diagram

20.3 In-Line Powered Device Detection (Cisco Method)

This section describes the flow process an Ethernet switch must perform in order to process in-line power requests made by a link partner (LP) capable of receiving in-line power.

1. The in-line powered device detection mode is enabled on each PHY through the serial management interface by setting MII Register bit 23E.10 = 1 and ensuring Auto-Negotiation Enable Bit (MII Register 0.12) = 1. The PHY will then start sending a special Fast Link Pulse (FLP) signal to the LP. MII Register 23E.9:8 will equal 00 during the search for devices needing in-line power.
2. The PHY monitors for the special FLP signal looped back by the LP. An LP device capable of receiving in-line power will loopback the special FLP pulses when it is in a powered-down state. This is reported when MII Register 23E.9:8 = 01. This can be verified as an in-line power detection interrupt by reading MII Register 26.9 = 1, which will subsequently be cleared and the interrupt de-asserted after the read. If an LP device does not loopback the special FLP after a specific time, then MII Register 23E.9:8 = 10.
3. If the PHY reports that the LP needs in-line power then the Ethernet switch needs to enable in-line power on this port externally of the PHY.
4. The PHY automatically disables in-line powered device detection after Event #3 above and now changes to the normal Auto-negotiation process. A link is then auto-negotiated and established when the Link status is set (MII Register bit 1.2 = 1)
5. In the event of a link down event (MII Register bit 1.2 = 0), the in-line power should be disabled to the in-line powered device external to the PHY. The PHY will disable the normal auto-negotiation process and re-enable in-line powered device detection mode.

20.4 IEEE 802.3af (DTE Power via MDI)

The VSC8244 is fully compatible with switch designs which are intended for use in systems that supply power to the DTE (Data Terminal Equipment) via the MDI (Media Dependent Interface, or twisted pair cable), as specified by IEEE 802.3af standard (Clause 33).

21 Advanced Test Modes

21.1 Ethernet Packet Generator (EPG)

For system-level debugging and in-system production testing, the VSC8244 includes an Ethernet packet generator for 1000BASE-T testing. This can be used to isolate problems between the MAC and PHY and between a local PHY and remote link partner. It is intended for use with lab testing equipment or in-system test equipment only, and should not be used when the VSC8244 is connected to a live network.

To use the EPG, it must be enabled by writing a “1” to MII Register 29E.15. This effectively disables all MAC-interface transmit pins and selects the EPG as the source for all data transmitted onto the VSC8244 twisted pair interface. For this reason, packet loss will occur if the EPG is enabled during transmission of packets from MAC to PHY. The MAC receive pins will still be active when the EPG is enabled, however. If it is necessary to disable the MAC receive pins as well, this can be done by writing a “1” to MII Register bit 0.10.

When a “1” is written to MII Register Bit 29E.14, the VSC8244 will begin transmitting IEEE802.3 layer-2 compliant packets with a data pattern of repeating 16-bit set by MII Register 30E. The source and destination addresses for each packet, packet size, interpacket gap, FCS state and transmit duration can all be controlled through MII Register 29E. Note that if MII Register Bit 29E.13 is cleared, MII Register Bit 29E.14 will be cleared automatically after 30,000,000 packets have been transmitted.

21.2 CRC Counter

A bad-CRC counter is also available for all incoming packets for 1000BASE-T mode. This counter is available in MII Register Bits 23E.7:0 - 1000BT CRC Counter and is automatically cleared when read.

21.3 Far-end Loopback

Far-end loopback mode when enabled (MII Register bit 23.3 = 1) forces incoming data from a link partner on the current media interface to be retransmitted back to the link partner on the media interface as shown in Figure 21. In addition, the incoming data will also appear on the receive data pins of the MAC interface. Data present on the transmit data pins of the MAC interface are ignored in this mode. For more information, please refer to MII Register 23.

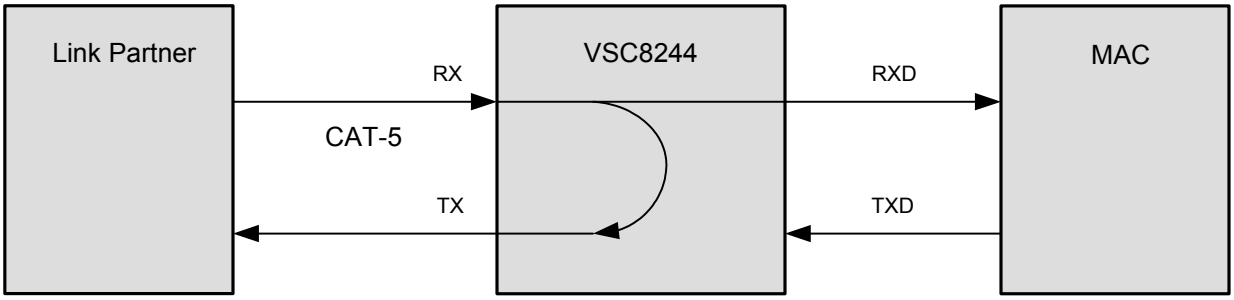


Figure 21. Far-end Loopback Block Diagram

21.4 Near-end Loopback

When Near-end loopback is set (MII Register bit 0.14 = 1), the Transmit Data (TXD) on the MAC interface is looped back onto the Receive Data (RXD) pins to the MAC as shown in Figure 22. In this mode, no signal is transmitted over the network media.

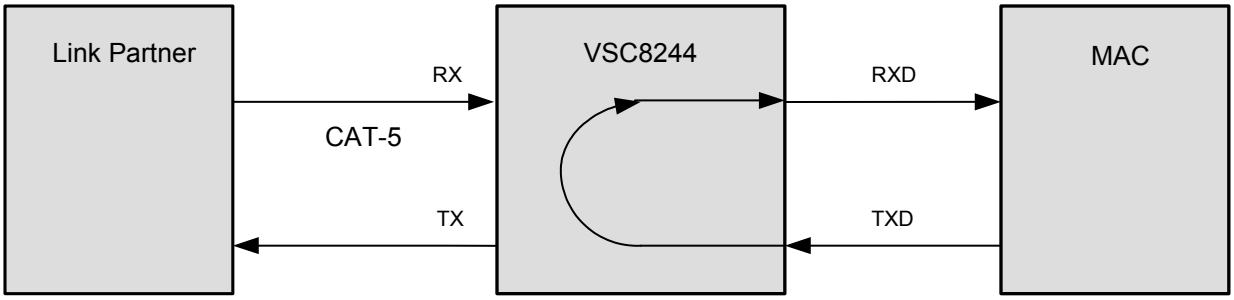


Figure 22. Near-end Loopback Block Diagram

21.5 Connector Loopback

Connector Loopback allows for the twisted pair interface to be looped back externally. In this mode, the PHY must be connected to a loopback connector or a loopback cable. For this loopback, pair A should be connected to pair B and pair C to pair D. This loopback will work in all speeds selected for the interface.

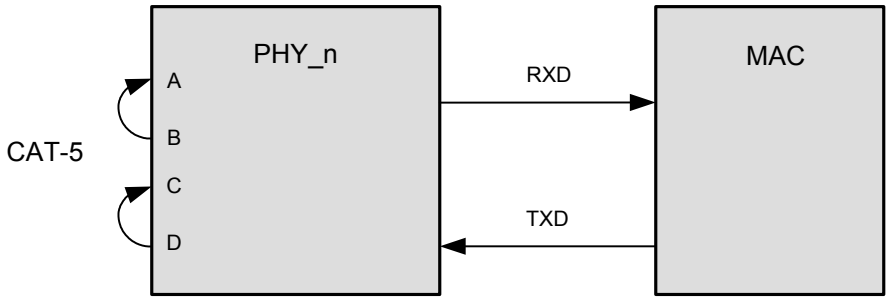


Figure 23. Connector Loopback

The autonegotiation, speed, and duplex can be configured using MII registers 0, 4, and 9. For 1000BT connector loopback only the following additional writes are required in the specified order.

1. Master/Slave configuration forced to master (MII Register Bits 9.12:11 = 11)
2. Enable 1000BT connector loopback (MII Register Bit 24.0 = 1)
3. Disable pair swap correction (MII Register Bit 18.5 = 1)
4. Disable autonegotiation and force 1000BT link (MII Register Bit 0.12 = 0, MII Register Bit 0.6 = 1, and MII Register Bit 0.13 = 0) and force either full or half duplex (MII Register Bit 0.8 = 0 or 1).

22 Initialization & Configuration

22.1 Resets

There are four conditions which can cause a reset of some or all parts of the VSC8244:

Device Power-up: On device power-up, the VSC8244 first reads the status of the CMODE hardware configuration and sets the appropriate MII register bits. All MII register bits not associated to a CMODE hardware configuration are then reset to their default values. The last step in power-up before the device becomes active is a read of EEPROM configuration, if an EEPROM is present. Note that because it is the last step in the reset sequence, it is possible for the EEPROM to overwrite MII register bits previously set by CMODE hardware configuration.

Device Hardware Reset: A complete hardware reset of all four PHYs in the VSC8244 occurs on the rising edge of the $\overline{\text{RESET}}$ pin. This functions identically to device power-up, above.

Device Software Reset: A complete software reset of all four PHYs in the VSC8244 occurs on the rising edge of the $\overline{\text{SOFT\_RESET}}$ pin. When this occurs, all MII register bits not marked as "sticky" will be reset to their default values. If MII Register Bit 21E.14 is set to a "1", the EEPROM configuration data will be read next, if one is present.

PHY Software Reset through MII Register Bit 0.15: An individual PHY reset can be initiated by writing a "1" to MII Register Bit 0.15. This functions identically to device software reset, except that it only affects a single PHY in the VSC8244.

22.2 Power-Up Sequence

The power supply sequence to the VSC8244 may be powered in any order.

22.3 CMODE Pin Configuration

Eight CMODE (configuration mode) pins are used by the device to provide a flexible method of hardware configuration without the need for a microcontroller or station manager. Each CMODE pin maps to four configuration bits giving one pin control of 16 possible default settings. This is controlled by connecting the CMODE pins to either VDD33 or VSSS (ground) through an external 1% resistor as shown in Table 28. As a result, 32 total configuration bits settings at power-up are possible within the 8 CMODE pins as shown in Table 27.

The resistors used on the CMODE pins can be considered optional for designs that have access to the VSC8244's management interface. In this manner all configurations present in CMODE can be altered via MII register settings and the CMODE pins can be pulled to VSSS (ground). However, the only feature that still requires CMODE configuration is the PHYADDR[4:2] selection. This can be set by either tieing these pins to VDD33 or VSSS.

22.3.1 CMODE Hardware Configuration Bits

32 CMODE hardware configuration bits are mapped to the 8 CMODE pins as shown in the following table:

Table 27. CMODE Hardware Configuration Bits

CMODE pin #	Bit 3 Function (MSB)	Bit 2 Function	Bit 1 Function	Bit 0 Function (LSB)
7	RGMII Clock Skew[1]	Always set to logic “0”	ActiPHY	Link Speed Downshift
6	RGMII Clock Skew[0]	Always set to logic “0”	LED Combine Link/Act	LED Pulse-stretch/Blink
5	PHY Address [4]	Always set to logic “0”	LED Combine Link10/ 100/1000/Act	LED Combine COL/DUP
4	PHY Address [3]	Speed/Dup modes [1]	LED4[1]	LED4[0]
3	PHY Address[2]	Speed/Dup modes [0]	LED3[1]	LED3[0]
2	MAC interface [2]	Always set to logic “0”	LED2[1]	LED2[0]
1	MAC interface [1]	Pause Control[1]	LED1[1]	LED1[0]
0	Always set to logic “1”	Pause Control[0]	LED0[1]	LED0[0]

22.3.2 Setting the CMODE Configuration Bits

The CMODE pins are set by connecting the CMODE pins to either VDD33 or VSSS (ground) through an external 1% resistor. To set the CMODE pins to utilize the 32 CMODE configuration bits, please refer to the following combination table below:

Table 28. CMODE Pin Combinations

CMODE bit 3 value	CMODE bit 2 value	CMODE bit 1 value	CMODE bit 0 value	CMODE Resistor Value	Tied to VDD or GND
0	0	0	0	0	GND
0	0	0	1	2.26k	GND
0	0	1	0	4.02k	GND
0	0	1	1	5.90k	GND
0	1	0	0	8.25k	GND
0	1	0	1	12.1k	GND
0	1	1	0	16.9k	GND
0	1	1	1	22.6k	GND
1	0	0	0	0	VDD33
1	0	0	1	2.26k	VDD33
1	0	1	0	4.02k	VDD33
1	0	1	1	5.90k	VDD33
1	1	0	0	8.25k	VDD33
1	1	0	1	12.1k	VDD33
1	1	1	0	16.9k	VDD33
1	1	1	1	22.6k	VDD33

22.3.3 Hardware Configuration Bit Description

The function for each CMODE configuration bit shown in Table 27 is described in the following table:

Table 29. CMODE Configuration Bits

Name	Sets MII Register	Value	Description
MAC-side interface select [2:1]	23.14:12, 23.2:1	11	RGMII to CAT5
		10	Reserved
		01	Reserved
		00	RTBI to CAT5 (Please refer to Register 23 for additional settings required).
PHY Address [4:2]	N/A	xxx	3 MSBs of PHY address
ActiPHY™	28.6	1	Enable ActiPHY™ power management
		0	Disable ActiPHY™ power management
LEDn[1:0]	27.15:6	xx	Mapped directly to the two function selection bits for each LED pin. (see MII Register 27 for more information)
LED Pulse-Stretch/Blink Select	27.3	1	Collision, Activity, Rx and Tx LED outputs will be pulse-stretched when active
		0	Collision, Activity, Rx and Tx LED outputs will blink when active
LED combine Link with Activity	27.2	1	Link LEDs indicate link status only
		0	Link LEDs will blink or flash when activity is present. Blink/flash behavior is selected by Pulse-Stretch Enable bit.
LED combine Link10/100/1000 with Activity	27.1	1	Link10, Link100, Link1000, Link10/100, Link100/1000 LEDs indicate link status only
		0	Link10, Link100, Link1000, Link10/100, Link100/1000 LEDs will blink or flash when activity is present. Blink/flash behavior is selected by Pulse-Stretch Enable bit.
LED combine Collision with Duplex	27.0	1	Duplex LED indicates duplex status only
		0	Duplex LED will blink or flash when collision is present. Blink/flash behavior is selected by Pulse-Stretch Enable bit.
Speed/Duplex autonegotiation advertisement	4.8:5, 9.9:8	11	10/100BASE-T, HDX, FDX
		10	1000BASE-T, FDX
		01	10/100/1000BASE-T, FDX; 10/100BASE-T HDX
		00	10/100/1000BASE-T, HDX, FDX
Link Speed Downshift	20E.4	1	Enable link speed downshift capability on 2-pair cable or after 3 failed autonegotiation attempts
		0	Link only according to autonegotiation resolution
Pause control [1:0]	4.11:10	xx	Pause Control autonegotiation advertisement
RGMII Skew [1:0][1]	23.11:8	11	2.5ns skew on RX_CLK and TX_CLK
		10	2ns skew on RX_CLK and TX_CLK
		01	1.5ns skew on RX_CLK and TX_CLK
		00	No skew on RX_CLK and TX_CLK

[1] To independently control the RX_CLK and TX_CLK RGMII skew please refer to MII Register 23 for more information.

22.4 EEPROM Interface

The optional EEPROM interface on the VSC8244 provides the PHY with the ability to self configure its internal registers. The EEPROM is read on powerup or deassertion of RESET. The EEPROM can also be accessed through MII registers for field configurability.

The optional EEPROM must have a two-wire interface such as Atmel "AT24CXXX" in order to interface to the VSC8244. As defined by this interface, data is clocked from the VSC8244 on the falling edge of EECLK. The VSC8244 determines that an external EEPROM is present by monitoring the EEDAT pin at powerup or when RESET is de-asserted. If EEDAT is connected to a 4.7kΩ external pull-up resistor, the VSC8244 assumes an EEPROM is present. The EEDAT pin can be left floating or grounded to indicate no EEPROM. If the VSC8244 detects an EEPROM present, then MII Register Bit 23.0 = 1 otherwise it will be cleared.

22.4.1 EEPROM Contents Description

If an EEPROM is present, the start-up control block looks for a “Vitesse Header” 0xBDBD at address 0 & 1 of the EEPROM. The address is incremented by 256 until the Vitesse Header is found. If the Vitesse Header is not found, or no EEPROM is connected, the VSC8244 bypasses the EEPROM read step.

Once the 'header value' is found, then the following two byte address values indicates the EEPROM word address where the configuration contents for the VSC8244 are located. At the base address location the next 10 bytes indicate where the configuration data contents to be programmed into the VSC8244 are located. The first address points to the data common to all PHYs. Each subsequent address location points to each individual PHY’s configuration contents. At each programming location the two bytes represent the total number of bytes (11 bits long, with MSB first) where Total_Number_Bytes[10:0] = number of SMI writes x 3 (1 byte for SMI port & reg address & 2 bytes for data). Refer to table below. Data is read from the EEPROM sequentially (at 50 Khz, or 50 kbits/s) until all SMI write commands are completed.

If an EEPROM is present, but the EEPROM does not acknowledge (according to the ATMEL EEPROM protocol), the VSC8244 waits for an acknowledge for approximately 3 seconds. If there is no acknowledge for 3 seconds, the VSC8244 will abort and continue into normal operation.

Table 30. EEPROM Configuration Contents

10-bit Address	Contents (bits 7:0)
0	0xBD
1	0xBD
2	PHY_ADDR[4:2], 00, Base_Address_Location[10:8]
3	Base_Address_Location[7:0] (K)
----------	----------
----------	----------
K	00000, Common_Config_Base_Address[10:8]
K+1	Common_Config_Base_Address[7:0] (X)
K+2	00000, PHY0_Specific_Config_Base_Address[10:8]
K+3	PHY0_Specific_Config_Base_Address[7:0] (Y)
K+4	00000, PHY1_Specific_Configuration_Address[10:8]
K+5	PHY1_Specific_Config_Base_Address[7:0]
K+6	00000, PHY2_Specific_Config_Base_Address[10:8]
K+7	PHY2_Specific_Config_Base_Address[7:0]
K+8	00000, PHY3_Specific_Config_Base_Address[10:8]
K+9	PHY3_Specific_Config_Base_Address[7:0]
----------	----------

Table 30. EEPROM Configuration Contents *(continued)*

10-bit Address	Contents (bits 7:0)
----------	----------
X	00000, Total_Number_Bytes[10:8]
X+1	Total_Number_Bytes[7:0] (M)
X+2	Register Address a
X+3	Data [15:8] to be written to Register Address a
X+4	Data [7:0] to be written to Register Address a
X+5	Register Address b
X+6	Data [15:8] to be written to Register Address b
X+7	Data [7:0] to be written to Register Address b
----------	----------
X+(M-2)	Register Address x
X+(M-1)	Data [15:8] to be written to Register Address x
X+M	Data [7:0] to be written to Register Address x
----------	----------
----------	----------
Y	00000, Total_Number_Bytes[10:8]
Y+1	Total_Number_Bytes[7:0] (N)
Y+2	Register Address a
Y+3	Data [15:8] to be written to Register Address a
Y+4	Data [7:0] to be written to Register Address a
----------	----------
Y+(N-2)	Register Address x
Y+(N-1)	Data [15:8] to be written to Register Address x
Y+N	Data [7:0] to be written to Register Address x
----------	----------
----------	----------
Max Address	----------

22.4.2 Programming Multiple VSC8244 using the same EEPROM

When the same EEPROM is used to initialize multiple VSC8244 devices, to prevent contention on the 2 wire bus, the EEPROM start-up block of each VSC8244 will monitor the bus for (PhyAddress[4:2] + 1)* 9 clock cycles for no bus activity and only then attempt to access the bus. PhyAddress[4:2] is chosen because these are the PhyAddress bits that are unique to each VSC8244. (i.e VSC8244s with lower PhyAddress get priority in the bus.)

NOTE: It is important that multiple VSC8244's REFCLK pins use the same clock. In addition, all VSC8244's $\overline{\text{RESET}}$ pins be asserted and deasserted simultaneously to ensure that the reference clock modes within each device are correctly set. This prevents having one VSC8244 use the output of a $CLK125_{MAC}$ or $CLK125_{micro}$ pin from another VSC8244 as a clock reference if the devices are sharing the same EEPROM.

Note: The above scheme for preventing bus contention will work only when multiple VSC8244 devices accessing the EEPROM have unique PhyAddress[4:2] values.

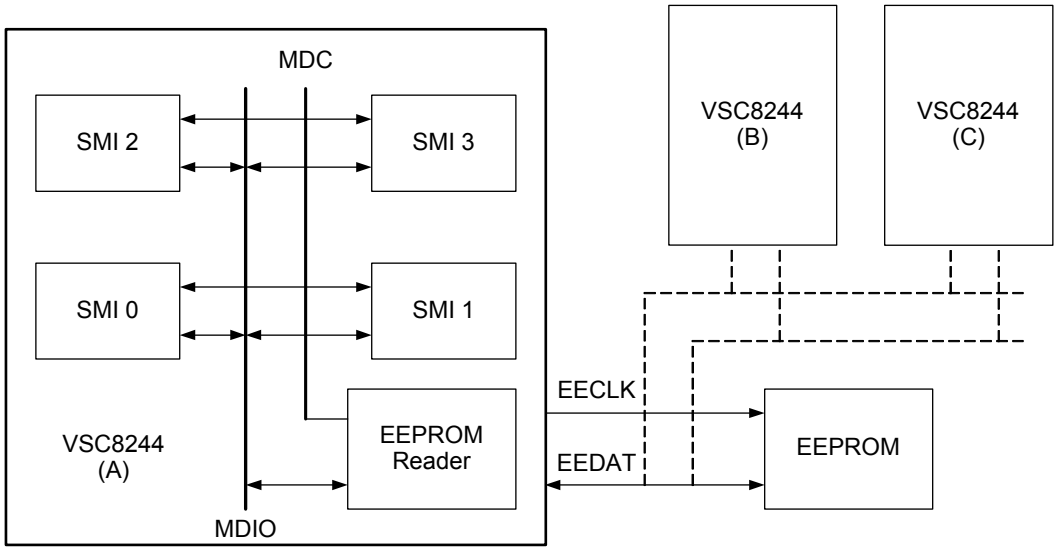


Figure 24. VSC8244 Devices Connected to use the same Startup EEPROM

Table 31. EEPROM Configuration Contents for Multiple VSC8244 Devices

10-bit Address	Contents (bits 7:0)
0	0xBD
1	0xBD
2	PHY_ADDR[4:2], 00, Base_Address_Location[10:8]
3	Base_Address_Location[7:0] (For VSC8244 A)
4	PHY_ADDR[4:2], 00, Base_Address_Location[10:8]
5	Base_Address_Location[7:0] (For VSC8244 B)
6	PHY_ADDR[4:2], 00, Base_Address_Location[10:8]
7	Base_Address_Location[7:0] (For VSC8244 C)
----------	----------
----------	----------
A	00000, Common_A_Config_Base_Address[10:8]
A+1	Common_A_Config_Base_Address[7:0] (X)
A+2	00000, PHY0_A_Specific_Config_Base_Address[10:8]
A+3	PHY0_A_Specific_Config_Base_Address[7:0]
A+4	00000, PHY1_A_Specific_Configuration_Address[10:8]
A+5	PHY1_A_Specific_Config_Base_Address[7:0]
A+6	00000, PHY2_A_Specific_Config_Base_Address[10:8]
A+7	PHY2_A_Specific_Config_Base_Address[7:0]
A+8	00000, PHY3_A_Specific_Config_Base_Address[10:8]
A+9	PHY3_A_Specific_Config_Base_Address[7:0]
----------	----------
----------	----------

Table 31. EEPROM Configuration Contents for Multiple VSC8244 Devices *(continued)*

10-bit Address	Contents (bits 7:0)
B	00000, Common_B_Config_Base_Address[10:8]
B+1	Common_B_Config_Base_Address[7:0] (Y)
B+2	00000, PHY0_B_Specific_Config_Base_Address[10:8]
B+3	PHY0_B_Specific_Config_Base_Address[7:0]
B+4	00000, PHY1_B_Specific_Configuration_Address[10:8]
B+5	PHY1_B_Specific_Config_Base_Address[7:0]
B+6	00000, PHY2_B_Specific_Config_Base_Address[10:8]
B+7	PHY2_B_Specific_Config_Base_Address[7:0]
B+8	00000, PHY3_B_Specific_Config_Base_Address[10:8]
B+9	PHY3_B_Specific_Config_Base_Address[7:0]
----------	----------
----------	----------
C	00000, Common_C_Config_Base_Address[10:8]
C+1	Common_C_Config_Base_Address[7:0] (Z)
C+2	00000, PHY0_C_Specific_Config_Base_Address[10:8]
C+3	PHY0_C_Specific_Config_Base_Address[7:0]
C+4	00000, PHY1_C_Specific_Configuration_Address[10:8]
C+5	PHY1_C_Specific_Config_Base_Address[7:0]
C+6	00000, PHY2_C_Specific_Config_Base_Address[10:8]
C+7	PHY2_C_Specific_Config_Base_Address[7:0]
C+8	00000, PHY3_C_Specific_Config_Base_Address[10:8]
C+9	PHY3_C_Specific_Config_Base_Address[7:0]
----------	----------
----------	----------
X	00000, Total_Number_Bytes[10:8]
X+1	Total_Number_Bytes[7:0] (N)
X+2	Register Address a
X+3	Data [15:8] to be written to Register Address a
X+4	Data [7:0] to be written to Register Address a
X+5	Register Address b
X+6	Data [15:8] to be written to Register Address b
X+7	Data [7:0] to be written to Register Address b
----------	----------
X+(N-2)	Register Address x
X+(N-1)	Data [15:8] to be written to Register Address x
X+N	Data [7:0] to be written to Register Address x
----------	----------
----------	----------
Y	00000, Total_Number_Bytes[10:8]

Table 31. EEPROM Configuration Contents for Multiple VSC8244 Devices *(continued)*

10-bit Address	Contents (bits 7:0)
Y+1	Total_Number_Bytes[7:0] (M)
Y+2	Register Address a
Y+3	Data [15:8] to be written to Register Address a
Y+4	Data [7:0] to be written to Register Address a
Y+5	Register Address b
Y+6	Data [15:8] to be written to Register Address b
Y+7	Data [7:0] to be written to Register Address b
----------	----------
Y+(M-2)	Register Address x
Y+(M-1)	Data [15:8] to be written to Register Address x
Y+M	Data [7:0] to be written to Register Address x
----------	----------
----------	----------
Z	00000, Total_Number_Bytes[10:8]
Z+1	Total_Number_Bytes[7:0] (P)
Z+2	Register Address a
Z+3	Data [15:8] to be written to Register Address a
Z+4	Data [7:0] to be written to Register Address a
Z+5	Register Address b
Z+6	Data [15:8] to be written to Register Address b
Z+7	Data [7:0] to be written to Register Address b
----------	----------
Z+(P-2)	Register Address x
Z+(P-1)	Data [15:8] to be written to Register Address x
Z+P	Data [7:0] to be written to Register Address x
----------	----------
----------	----------
Max Address	----------

With the above scheme for EEPROM contents, if multiple VSC8244 devices are initialized in a similar way, the base address locations can each point to the same address location from the EEPROM. If they have to be initialized differently, then each base location will differ for each device and the data contents to be configured for each will be unique.

22.4.3 Read/Write Access to the EEPROM

The VSC8244 has the ability to read and write to an EEPROM (such as an ATMEL AT24CXXX) connected to the EECLK and EEDAT pins of the device. If it is required to be able to write to the EEPROM, please refer to the EEPROM's specific datasheet to ensure that write protection on the EEPROM is not set.

To read a value from a specific address of the EEPROM, first read MII Register Bit 21E.11 and ensure that it is set. After confirming this bit is set, write the address to be read to MII Register Bits 21E.10:0, set MII Register Bit 21E.12 = 1, and then set MII Register Bit 21E.13 = 1. Wait until 21E.11 = 1 and then read the 8-bit data value found at 22E.15:8 that contains the contents of the address just read by the PHY.

To write a value to a specific address of the EEPROM, first read MII Register Bit 21E.11 and ensure that it is set. After confirming this bit is set, write the address to be written to MII Register Bits 21E.10:0, set MII Register Bit 21E.12 = 0, the 8-bit value to be written to MII Register Bits 22E.7:0, and then set MII Register Bit 21E.13 = 1.

For successful read and write transactions always wait until 21E.11 = 1 before performing another EEPROM read or write operation.

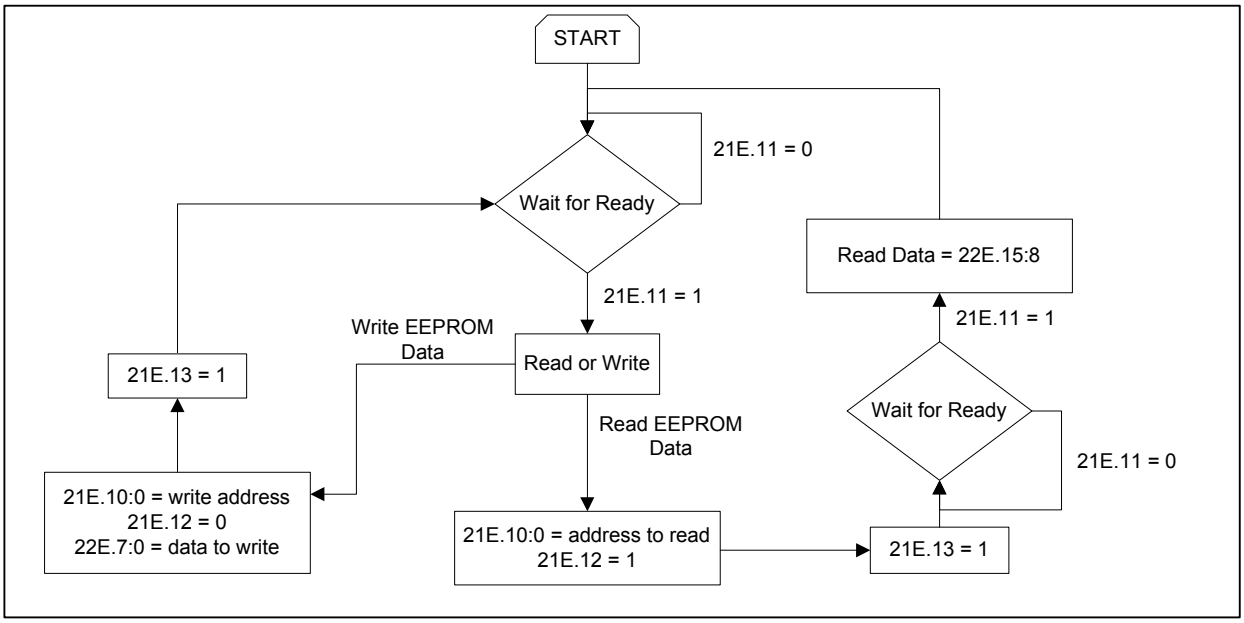


Figure 25. EEPROM Read and Write Register Flow

23 MII Register Set

The MII register map quick reference is listed on the following two pages:See “CMODE Pin Configuration” on page 52.

Table 32. MII Register Bit Modes

Register Bit Type	Description
S	“Sticky”[1] - this bit will retain value after a software reset and if MII Register 22.9 = 1
SS	“Super Sticky”[1] - this bit will retain value after a software reset
R/W	Read/Write bit
RO	Read Only bit
WO	Write Only bit
SC	Self-clearing bit
LL	This bit will latch the bit on low. The bit self-clears on read
LH	This bit will latch the bit on high. The bit self-clears on read
CMODE	Defined by CMODE pin settings

[1] “Sticky” refers to the behavior of the register bit(s) after a software reset. If an “S” appears in the sticky column, the corresponding bit(s) will retain their values after a software reset, as long as MII Register bit Register 22 (16h) – Extended Control & Status Register is set. If an “SS” appears in the sticky column, the corresponding bit(s) will retain their values after a software reset, regardless of the state of MII Register bit Register 22 (16h) – Extended Control & Status Register.

NOTE: For MII Registers 16-31 and Extended MII Registers 16E-30E, any bits marked as “Reserved” should be processed as read only and their states as undefined. In writing to registers with these reserved bits, one must perform a technique known commonly as “ready-modify write” where the entire register is read and only the intended bits to be changed are modified. These reserved bits cannot be changed and their read state cannot be considered static or unchanging.

23.1 MII Extended Page Registers

In order to provide additional functionality beyond the IEEE802.3 specified 32 MII registers, the VSC8244 contains an extended paging mode that allows an additional 15 registers. Access to the extended page registers (Registers 16E - 30E) is enabled by writing a “0001” to MII Register 31. When extended page register access is enabled, read/writes to MII registers 16 through 30 will affect the extended MII registers 16E through 30E. MII registers 0 through 15 are not affected by the state of the extended page register access. Writing a “0000” to MII Register 31 will restore normal MII register access.

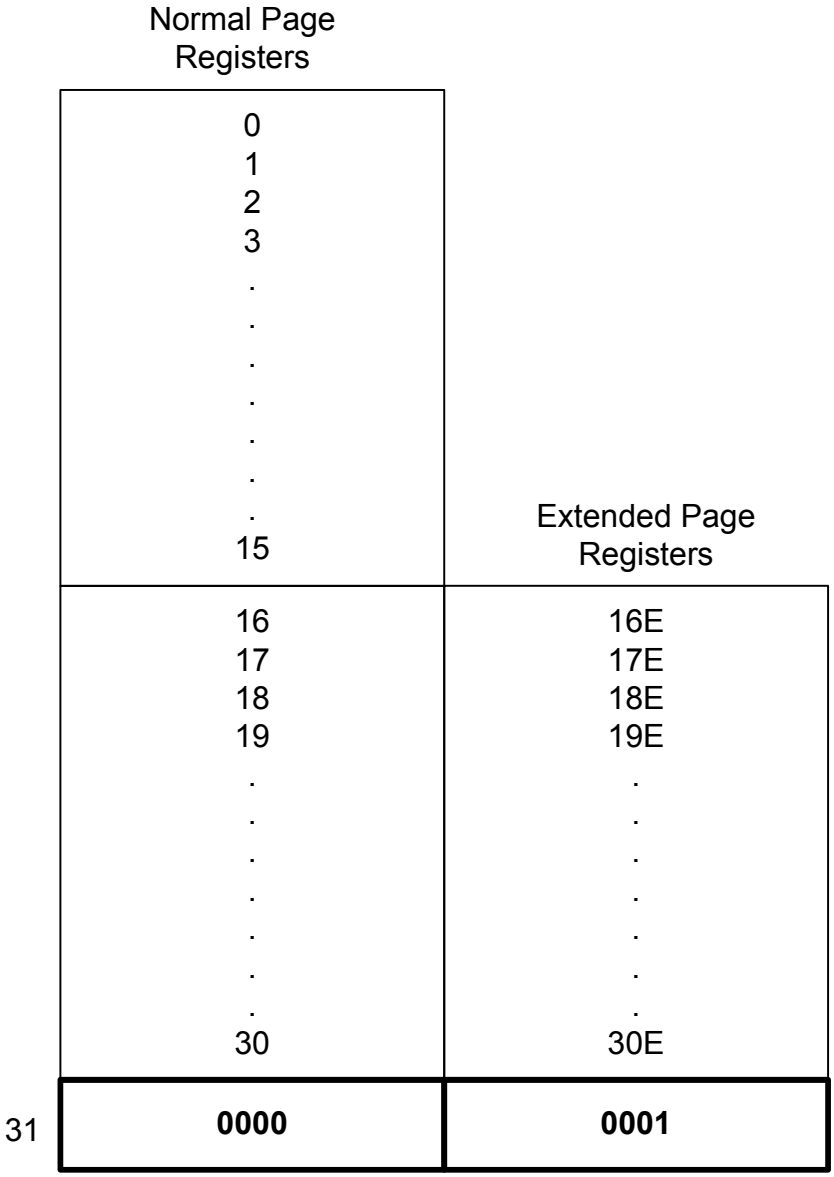


Figure 26. Extended Page Register

23.3 MII Register Quick Reference

Table 33. MII Register Quick Reference

Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0 (00h) Mode Control	Software Reset 0	Loopback 0	Forced Speed Select[0]	Auto-Neg Enable 1	Power-Down	Isolate 0	Restart Auto-Neg 0	Duplex Mode	Collision Test	Forced Speed Select[1]	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
1 (01h) Mode Status	100B-T4 0	100B-X FDX	100B-X HDX	10B-T FDX 1	10B-T HDX 1	100B-T2 FDX	100B-T2 HDX	Extended Status	Reserved 0	Preamble Suppression	Auto-Neg Complete 0	Remote Fault 0	Auto-Neg Capability 1	Link Status 0	Jabber Detect 0	Extended Capability 1
2 (02h) PHY Identifier #1	OUI_MSB[3]	OUI_MSB[4]	OUI_MSB[5]	OUI_MSB[6]	OUI_MSB[7]	OUI_MSB[8]	OUI_MSB[9]	OUI_MSB[10]	OUI_MSB[11]	OUI_MSB[12]	OUI_MSB[13]	OUI_MSB[14]	OUI_MSB[15]	OUI_MSB[16]	OUI_MSB[17]	OUI_MSB[18]
3 (03h) PHY Identifier #2	OUI_LSB[19]	OUI_LSB[20]	OUI_LSB[21]	OUI_LSB[22]	OUI_LSB[23	OUI_LSB[24]	Vendor Model Number[5]	Vendor Model Number[4]	Vendor Model Number[3]	Vendor Model Number[2]	Vendor Model Number[1]	Vendor Model Number[0]	Vendor Rev Number[3]	Vendor Rev Number[2]	Vendor Rev Number[1]	Vendor Rev Number[0]
4 (04h) Auto-Neg Advertisement	Next Page 0	Reserved 0	Remote Fault	Reserved 0	Asymmetric Pause CMODE	Symmetric Pause CMODE	100B-T4 0	100B-X FDX	100B-X HDX	10B-T FDX CMODE	10B-T HDX CMODE	Selector Field[4]	Selector Field[3]	Selector Field[2]	Selector Field[1]	Selector Field[0]
5 (05h) Auto-Neg Link Partner Ability	Next Page 0	ACK 0	Remote Fault	Reserved 0	Asymmetric Pause 0	Symmetric Pause 0	100B-T4 0	100B-X FDX	100B-X HDX	10B-T FDX 0	10B-T HDX 0	Selector Field[4]	Selector Field[3]	Selector Field[2]	Selector Field[1]	Selector Field[0]
6 (06h) Auto-Neg Expansion	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Parallel Detect Fault	LP NP Able 0	NP Able 1	Page Received	LP Auto-Neg Able 0
7 (07h) Auto-Neg NP Transmit	Next Page 0	Reserved 0	Message Page	ACK2 0	Toggle 0	Message/ Unformatted[10]	Message/ Unformatted[9]	Message/ Unformatted[8]	Message/ Unformatted[7]	Message/ Unformatted[6]	Message/ Unformatted[5]	Message/ Unformatted[4]	Message/ Unformatted[3]	Message/ Unformatted[2]	Messag/ Unformatted[1]	Message/ Unformatted[0]
8 (08h) Auto-Neg Link Partner NP Receive	LP Next Page	LP ACK 0	LP Message Page	LP ACK2 0	LP Toggle 0	LP Message/ Unformatted[10]	LP Message/ Unformatted[9]	LP Message/ Unformatted[8]	LP Message/ Unformatted[7]	LP Message/ Unformatted[6]	LP Message/ Unformatted[5]	LP Message/ Unformatted[4]	LP Message/ Unformatted[3]	LP Message/ Unformatted[2]	LP Message/ Unformatted[1]	LP Message/ Unformatted[0]
9 (09h) 1000BASE-T Control	Transmit Test[1]	Transmit Test[2]	Transmit Test[3]	M/S Config Enable 0	M/S Config Value 0	Port Type 1	1000B-T FDX	1000B-T HDX	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
10 (0Ah) 1000BASE-T Status	M/S Config Fault	M/S Config Resolution 1	Local Receiver Status	Remote Receiver Status	LP 1000B-T FDX 0	LP 1000B-T HDX 0	Reserved 0	Reserved 0	Idle Error Count[7] 0	Idle Error Count[6] 0	Idle Error Count[5] 0	Idle Error Count[4] 0	Idle Error Count[3] 0	Idle Error Count[2] 0	Idle Error Count[1] 0	Idle Error Count[0] 0
11 (0Bh) Reserved	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
12 (0Ch) Reserved	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
13 (0Dh) Reserved	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
14 (0Eh) Reserved	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
15 (0Fh) 1000BASE-T Status Extension	1000B-X FDX	1000B-X HDX	1000B-T FDX	1000B-T HDX	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
16 (10h) 100BASE-TX Status Extension	100B-TX Descrambler Locked 0	100B-TX Lock Error Detected	100B-TX Disconnect State 0	100B-TX Current Link Status 0	100B-TX Receive Error Detected	100B-TX Transmit Error Detected	100B-TX SSD Error Detected	100B-TX ESD Error Detected	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
17 (11h) 1000BASE-T Status Extension	1000B-T Descrambler Locked 0	1000B-T Lock Error Detected	1000B-T Disconnect State 0	1000B-T Current Link Status	1000B-T Receive Error Detected	1000B-T Transmit Error Detected	1000B-T SSD Error Detected	1000B-T ESD Error Detected	1000B-T Carrier Extension Error	Non-compliant BCM5400 Detected	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
18 (12h) Bypass Control	Transmit Disable 0	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved 0	1000BT Transmitter Test Clock Enable	Reserved --	Reserved --	Disable Automatic Pair Swap Correction	Disable Polarity Correction	Parallel-Detect Control	Reserved --	Disable Auto 1000B-T NP	125MHz Clock Output Enable
19 (13h) Reserved	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
20 (14h) Reserved	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
21 (15h) Reserved	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
22 (16h) Extended Control & Status	Link Disable	Jabber Detect Disable	10B-T/ 100B-TX Echo Disable	Reserved --	Squelch[1] 0	Squelch[0] 0	Sticky Reset Enable	EOF Error Detected 0	10B-T Disconnect 0	10B-T Link Status 0	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
23 (17h) Extended PHY Control #1	Reserved --	MAC I/F Mode[2] 0	MAC I/F Mode[1] 0	MAC I/F Mode[0] 0	RGMII TX_CLK Skew Seletction	RGMII TX_CLK Skew Seletction	RGMII RX_CLK Skew Seletction	RGMII RX_CLK Skew Seletction	Reserved --	Reserved --	RX Idle Clock Enable	Reserved --	Far End Loopback Mode Enable	MAC/ Media Mode Select	MAC/ Media Mode Select	EEPROM Status

Table 33. MII Register Quick Reference *(continued)*

Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24 (18h) Extended PHY Control #2	100/ 1000B-TX Edge Rate[2]	100/ 1000B-TX Edge Rate[1]	100/ 1000B-TX Edge Rate[0]	Enable PICMG 2.16 Miser Mode	Reserved --	Reserved --	TX FIFO Depth[2] (RGMII) 1	TX FIFO Depth[1] (RGMII) 0	TX FIFO Depth[0] (RGMII) 0	RX FIFO Depth[2] (RTBI)	RX FIFO Depth[1] (RTBI)	RX FIFO Depth[0] (RTBI)	Reserved --	Reserved --	Reserved --	1000BT Connector Loopback 0
25 (19h) Interrupt Mask	Interrupt Pin Enable 0	Speed State-Change Interrupt	Link State-Change Interrupt Mask	Duplex State-Change Interrupt	Auto-Neg Error Interrupt Mask	Auto-Neg-Done Interrupt Mask	In-line Powered Device Detected	Symbol Error Interrupt Mask	Descrambler Lock-Lost Interrupt	TX FIFO Interrupt Mask	RX FIFO Interrupt Mask	Reserved --	False Carrier Interrupt Mask	Cable Impaired-Detect Interrupt	MASTER/ SLAVE Interrupt Mask	RX_ER Interrupt Mask
26 (1Ah) Interrupt Status	Interrupt Status	Speed State-Change Interrupt	Link State-Change Interrupt Status	FDX State-Change Interrupt Status	Auto-Neg Error Interrupt Status	Auto-Neg-Done Interrupt Status	In-line Powered Device Interrupt	Symbol Error Interrupt Status	Descrambler Lock-Lost Interrupt	TX FIFO Interrupt Status	RX FIFO Interrupt Status	Reserved --	False Carrier Interrupt Status	Cable Impaired-Detect Interrupt	MASTER/ SLAVE Interrupt Status	RX_ER Interrupt Status
27 (1Bh) Serial LED Control	LED Pin 4 Config CMODE	LED Pin 4 Config CMODE	LED Pin 3 Config CMODE	LED Pin 3 Config CMODE	LED Pin 2 Config CMODE	LED Pin 2 Config CMODE	LED Pin 1 Config CMODE	LED Pin 1 Config CMODE	LED Pin 0 Config CMODE	LED Pin 0 Config CMODE	LED Pulse-stretch Rate/Blink Rate	LED Pulse-stretch Rate/Blink Rate	LED Pulse-stretch/ Blink Select	LED Pulsing Behavior	LED Link/ Activity Behavior	LED Duplex/ Collision Behavior
28 (1Ch) Auxiliary Control & Status	Auto-Neg Complete 0	Auto-Neg Disabled 0	MDI/MDI-X XOver Indication	CD Pair Swap	A Polarity Inversion 0	B Polarity Inversion 0	C Polarity Inversion 0	D Polarity Inversion 0	Reserved --	Enhanced ActiPHY Enable	FDX Status 0	Speed Status[1]	Speed Status[0]	Reserved --	ActiPHY Sleep Timer	ActiPHY Sleep Timer
29 (1Dh) Reserved	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
3-- (1Eh) Reserved	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
31 (1Fh) Extended Page Acess	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Extended Page Access

Key: Bit Name (Read/ Writable) Bit Name (Read Only)

23.4 MII Register Quick Reference - Extended Page Mode

Table 34. MII Register Quick Reference - Extended Page Mode

Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
16E (10h) Remote Fault Control & Status	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
17E (11h) $CLK125_{micro}$ Clock	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	CLK125micro Enable
18E (12h) Reserved	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
19E (13h) Reserved	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
20E (14h) Extended PHY Control #3	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	CLK125micro Frequency	Reserved --	Reserved --	Reserved --	Enable Link Speed Auto-	Link Speed Auto-downshift	Link Speed Auto-downshift	Link Speed Auto-downshift	Reserved --
21E (15h) EEPROM Status & Control	Reserved --	Re-read EEPROM on software	EEPROM Access Enable	EEPROM Read/ Write	EEPROM Ready 1	EEPROM Address 0	EEPROM Address 0	EEPROM Address 0	EEPROM Address 0	EEPROM Address 0	EEPROM Address 0	EEPROM Address 0	EEPROM Address 0	EEPROM Address 0	EEPROM Address 0	EEPROM Address 0
22E (16h) EEPROM Data Read/Write	EEPROM Read Data 0	EEPROM Read Data 0	EEPROM Read Data 0	EEPROM Read Data 0	EEPROM Read Data 0	EEPROM Read Data 0	EEPROM Read Data 0	EEPROM Read Data 0	EEPROM Write Data 0	EEPROM Write Data 0	EEPROM Write Data 0	EEPROM Write Data 0	EEPROM Write Data 0	EEPROM Write Data 0	EEPROM Write Data 0	EEPROM Write Data 0
23E (17h) Extended PHY Control #4	PHY Address	PHY Address	PHY Address	PHY Address	PHY Address	Enable Device Detection	Device Detection Status	Device Detection Status	CRC Counter	CRC Counter	CRC Counter	CRC Counter	CRC Counter	CRC Counter	CRC Counter	CRC Counter
24E (18h) Reserved	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
25E (19h) Reserved	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
26E (1Ah) Reserved	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
27E (1Bh) Reserved	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
28E (1Ch) Reserved	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --	Reserved --
29E (1Dh) 1000BASE-T EPG #1	EPG Enable	EPG Run/ Stop	Transmission Duration	Packet Length	Packet Length	Inter-packet Gap	Destination Address 0	Destination Address 0	Destination Address 0	Destination Address 1	Source Address	Source Address	Source Address	Source Address	Reserved --	Bad FCS Generation
30E (1Eh) 1000BASE-T EPG #2	EPG Packet Payload	EPG Packet Payload	EPG Packet Payload	EPG Packet Payload	EPG Packet Payload	EPG Packet Payload	EPG Packet Payload	EPG Packet Payload	EPG Packet Payload	EPG Packet Payload	EPG Packet Payload	EPG Packet Payload	EPG Packet Payload	EPG Packet Payload	EPG Packet Payload	EPG Packet Payload

Key: Bit Name (Read/ Writable) Bit Name (Read Only)

24 MII Register Descriptions

Registers 0-15 comply with the IEEE 802.3 standard. Enhancements beyond the specification are noted within each of these registers. For more information on normal operation of registers 0-15, please consult with the IEEE standard.

24.1 Register 0 (00h) – Mode Control Register

Register 0 (00h) – Mode Control Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	Software Reset[1]	R/W SC	1 = Reset asserted 0 = Reset de-asserted	0
14	Loopback[2]	R/W	1 = Loopback on 0 = Loopback off	0
6, 13	Forced Speed Selection	R/W	00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved	10
12	Auto-Negotiation Enable	R/W	1 = Auto-Negotiation enabled 0 = Auto-Negotiation disabled	1
11	Power-Down	R/W	1 = Power-down 0 = Power-up	0
10	Isolate	R/W	1 = Disable RGMII/RTBI outputs 0 = Normal Operation	0
9	Restart Auto-Negotiation	R/W SC	1 = Restart MII 0 = Normal operation	0
8	Duplex Mode	R/W	1 = Full duplex 0 = Half duplex	0
7	Collision Test Enable	R/W	1 = Collision test enabled 0 = Collision test disabled	0
6	MSB for Speed Selection (see bit 13 above)	-	-	1
5:0	Reserved	-	-	000000

[1] A soft reset restores all SMI registers to their default states, except for registers marked with an “S” or “SS” in the sticky column. After setting this bit, the user needs to wait 4 microseconds to initiate the next SMI access.

[2] The loopback mechanism works in the current speed and duplex mode of operation. If the link is down the operating mode is determined by bits 0.13 and 0.6 (forced speed selection) and 0.8.

24.2 Register 1 (01h) – Mode Status Register

Register 1 (01h) – Mode Status Register

Bit	Name	Access	States	Reset Value
15	100BASE-T4 Capability	RO	1 = 100BASE-T4 capable	0
14	100BASE-TX FDX Capability	RO	1 = 100BASE-TX FDX capable	1
13	100BASE-TX HDX Capability	RO	1 = 100BASE-TX HDX capable	1
12	10BASE-T FDX Capability	RO	1 = 10BASE-T FDX capable	1
11	10BASE-T HDX Capability	RO	1 = 10BASE-T HDX capable	1
10	100BASE-T2 FDX Capability	RO	1 = 100BASE-T2 FDX capable	0
9	100BASE-T2 HDX Capability	RO	1 = 100BASE-T2 HDX capable	0
8	Extended Status Enable	RO	1 = Extended status information present in R15	1
7	Reserved	RO		0
6	Preamble Suppression Capability	RO	1 = MF preamble may be suppressed 0 = MF preamble always required	1
5	Auto-Negotiation Complete	RO	1 = Auto-Negotiation complete 0 = Auto-Negotiation not complete	0
4	Remote Fault	RO LH	1 = Far-end fault detected 0 = No fault detected	0
3	Auto-Negotiation Capability	RO	1 = Auto-Negotiation capable	1
2	Link Status[1]	RO LL	1 = Link is up 0 = Link is down	0
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No jabber condition detected	0
0	Extended Capability	RO	1 = Extended register capable	1

[1] If Link Status bit is equal to "1" and powerdown is subsequently set (MII Register 0.11 = 1), Link Status bit may not clear. To clear the bit in this scenario, write MII Register 0.11 = 1, then MII Register 0.11 = 0, and finally MII Register 0.11 = 1. This will ensure the Link Status bit is cleared when powerdown is enabled.

24.3 Register 2 (02h) – PHY Identifier Register #1

Register 2 (02h) – PHY Identifier Register #1

Bit	Name	Access	States	Reset Value
15:0	Organizationally Unique Identifier	RO	OUI most significant bits (Vitesse OUI bits 3:18)	0000000000001111 or (000Fh)

24.4 Register 3 (03h) – PHY Identifier Register #2

Register 3 (03h) – PHY Identifier Register #2

Bit	Name	Access	States	Reset Value
15:10	Organizationally Unique Identifier	RO	OUI least significant bits (Vitesse OUI bits 19:24)	110001
9:4	Vendor Model Number	RO	Vendor's model number (IC)	101100 = VSC8244
3:0	Vendor Revision Number	RO	Vendor's revision number (IC)	0010 = Silicon Revision C

24.5 Register 4 (04h) – Auto-Negotiation Advertisement Register

Register 4 (04h) – Auto-Negotiation Advertisement Register

Bit	Name	Access	States	Reset Value
15	Next-Page Transmission Request	R/W	1 = Next-Page transmission request	0
14	Reserved	RO		0
13	Transmit Remote Fault	R/W	1 = Transmit remote fault	0
12	Reserved technologies	R/W		0
11	Advertise Asymmetric Pause	R/W	1 = Advertise Asymmetric Pause capable	CMODE
10	Advertise Symmetric Pause	R/W	1 = Advertise Symmetric Pause capable	CMODE
9	Advertise 100BASE-T4 Capability	R/W	1 = 100BASE-T4 capable	0
8	Advertise 100BASE-TX FDX	R/W	1 = 100BASE-TX FDX capable	CMODE
7	Advertise 100BASE-TX HDX	R/W	1 = 100BASE-TX HDX capable	CMODE
6	Advertise 10BASE-T FDX	R/W	1 = 10BASE-T FDX capable	CMODE
5	Advertise 10BASE-T HDX	R/W	1 = 10BASE-T HDX capable	CMODE
4:0	Advertise Selector Field	R/W		00001

24.6 Register 5 (05h) – Auto-Negotiation Link Partner Ability Register

Register 5 (05h) – Auto-Negotiation Link Partner Ability Register

Bit	Name	Access	States	Reset Value
15	LP Next-Page Transmit Request	RO	1 = LP NP transmit request	0
14	LP Acknowledge	RO	1 = LP acknowledge	0
13	LP Remote Fault	RO	1 = LP remote fault	0
12	Reserved	RO	-	0
11	LP Asymmetric Pause Capability	RO	1 = LP Advertise Asymmetric Pause capable	0
10	LP Symmetric Pause Capability	RO	1 = LP Advertise Symmetric Pause capable	0
9	LP Advertise 100BASE-T4 Capability	RO	1 = LP Advertise 100BASE-T4 capable	0
8	LP Advertise 100BASE-TX FDX	RO	1 = LP 100BASE-TX FDX capable	0
7	LP Advertise 100BASE-TX HDX	RO	1 = LP 100BASE-TX HDX capable	0
6	LP Advertise 10BASE-T FDX	RO	1 = LP 10BASE-T FDX capable	0
5	LP Advertise 10BASE-T HDX	RO	1 = LP 10BASE-T HDX capable	0
4:0	LP Advertise Selector Field	RO	LP Advertise Selector Field	00000

24.7 Register 6 (06h) – Auto-Negotiation Expansion Register

Register 6 (06h) – Auto-Negotiation Expansion Register

Bit	Name	Access	States	Reset Value
15:5	Reserved	RO		00000000000
4	Parallel Detection Fault	RO LH	1 = Parallel detection fault	0
3	LP Next-Page Able	RO	1 = LP Next-Page capable	0
2	Local PHY Next-Page Able	RO	1 = Next-Page capable	1
1	Page Received	RO LH	1 = New page has been received	0
0	LP Auto-Negotiation Able	RO	1 = LP Auto-Negotiation capable	0

24.8 Register 7 (07h) – Auto-Negotiation Next-Page Transmit Register

Register 7 (07h) – Auto-Negotiation Next-Page Transmit Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	Next Page	R/W	1 = More pages follow 0 = Last page	0
14	Reserved	RO		0
13	Message Page	R/W	1 = Message page 0 = Unformatted page	1
12	Acknowledge2	R/W	1 = Will comply with request 0 = Cannot comply with request	0
11	Toggle	RO	1 = Previous transmitted LCW == 0 0 = Previous transmitted LCW == 1	0
10:0	Message/Unformatted Code	R/W		00000000001

24.9 Register 8 (08h) – Auto-Negotiation Link Partner Next-Page Receive Register

Register 8 (08h) – Auto-Negotiation Link Partner Next-Page Receive Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	LP Next Page	RO	1 = More pages follow 0 = Last page	0
14	LP Acknowledge	RO	1 = LP acknowledge	0
13	LP Message Page	RO	1 = Message page 0 = Unformatted page	0
12	LP Acknowledge2	RO	1 = LP will comply with request	0
11	LP Toggle	RO	1 = Previous transmitted LCW == 0 0 = Previous transmitted LCW == 1	0
10:0	LP Message/Unformatted Code	RO		00000000000

24.10 Register 9 (09h) – 1000BASE-T Control Register

Register 9 (09h) – 1000BASE-T Control Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:13	Transmitter Test Mode	R/W	Described below, per IEEE 802.3, 40.6.1.1.2	000
12	MASTER/SLAVE Manual Configuration Enable	R/W	1 = Enable MASTER/SLAVE Manual Configuration value 0 = Disable MASTER/SLAVE Manual Configuration value	0
11	MASTER/SLAVE Manual Configuration Value	R/W	1 = Configure PHY as MASTER during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one. 0 = Configure PHY as SLAVE during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one.	0
10	Port Type	R/W	1 = Multi-port device 0 = Single-port device	1
9	1000BASE-T FDX Capability	R/W	1 = PHY is 1000BASE-T FDX capable	CMODE
8	1000BASE-T HDX Capability	R/W	1 = PHY is 1000BASE-T HDX capable	CMODE
7:0	Reserved	R/W		00000000

9.15:13 Transmitter/Receiver Test Mode

This test is valid only in 1000BASE-T mode. Refer to IEEE 802.3-2002, section 40.6.1.1.2 for more information.

Table 35. Transmitter/Receiver Test Mode

Bit 1 (9.15)	Bit 2 (9.14)	Bit 3 (9.13)	Test Mode
0	0	0	Normal operation
0	0	1	Test Mode 1 – Transmit waveform test
0	1	0	Test Mode 2 – Transmit jitter test in MASTER mode
0	1	1	Test Mode 3 – Transmit jitter test in SLAVE mode
1	0	0	Test Mode 4 – Transmitter distortion test
1	0	1	Reserved; operation not defined
1	1	0	Reserved; operation not defined
1	1	1	Reserved; operation not defined

- **Test Mode 1:** The PHY repeatedly transmits the following sequence of data symbols from all four transmitters: {{"+2" followed by 127 "0" symbols}, {"-2" followed by 127 "0" symbols}, {"+1" followed by 127 "0" symbols}, {"-1" followed by 127 "0" symbols}, {128 "+2" symbols, 128 "-2" symbols, 128 "+2" symbols, 128 "-2" symbols}, {1024 "0" symbols}}. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in MASTER timing mode.
- **Test Mode 2:** The PHY transmits the data symbol sequence {+2, -2} repeatedly on all channels. The transmitter should use a 125.00 MHz ± 0.01% clock in the MASTER timing mode.
- **Test Mode 3:** The PHY transmits the data symbol sequence {+2, -2} repeatedly on all channels. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in SLAVE timing mode.

- **Test Mode 4:** The PHY transmits the sequence of symbols generated by the following scrambler generator polynomial, bit generation, and level mappings:
  The maximum-length shift register used to generate the sequences defined by this polynomial is updated once per symbol interval (8ns). The bits stored in the shift register delay line at a particular time *n* are denoted by Scrn[10:0]. At each symbol period, the shift register is advanced by one bit, and one new bit represented by Scrn[0] is generated. Bits $Scr_n[8]$ and $Scr_n[10]$ are exclusive-OR'd together to generate the next $Scr_n[0]$ bit. The bit sequences, $x0_n$, $x1_n$, and $x2_n$, generated from combinations of the scrambler bits as shown in the following equations, shall be used to generate the quinary symbols, s_n, as shown in the following table. The transmitter should use a 125.00 MHz ± 0.01% clock and should operate in MASTER timing mode.

Table 36. Test Mode 4

$x2_n$	$x1_n$	$x0_n$	Quinary Symbol, s_n
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	-1
1	0	0	0
1	0	1	1
1	1	0	-2
1	1	1	-1

24.11 Register 10 (0Ah) – 1000BASE-T Status Register

Register 10 (0Ah) – 1000BASE-T Status Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	MASTER/SLAVE Configuration Fault	RO LH SC	1 = MASTER/SLAVE configuration fault detected 0 = No MASTER/SLAVE configuration fault detected	0
14	MASTER/SLAVE Configuration Resolution	RO	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	1
13	Local Receiver Status	RO	1 = Local receiver OK (loc_rcvr_status == OK) 0 = Local receiver not OK (loc_rcvr_status == NOT_OK)	0
12	Remote Receiver Status	RO	1 = Remote receiver OK (rem_rcvr_status == OK) 0 = Remote receiver not OK (rem_rcvr_status == NOT_OK)	0
11	LP 1000BASE-T FDX Capability	RO	1 = LP 1000BASE-T FDX capable 0 = LP not 1000BASE-T FDX capable	0
10	LP 1000BASE-T HDX Capability	RO	1 = LP is 1000BASE-T HDX capable 0 = LP is not 1000BASE-T HDX capable	0
9:8	Reserved	RO		00
7:0	Idle Error Count	RO SC		00000000

24.12 Register 11 (0Bh) – Reserved Register

Register 11 (0Bh) – Reserved Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:0	Reserved	RO		00000000 00000000

24.13 Register 12 (0Ch) – Reserved Register

Register 12 (0Ch) – Reserved Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:0	Reserved	RO		00000000 00000000

24.14 Register 13 (0Dh) – Reserved Register

Register 13 (0Dh) – Reserved Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:0	Reserved	RO		00000000 00000000

24.15 Register 14 (0Eh) – Reserved Register

Register 14 (0Eh) – Reserved Register				
Bit	**Name**	**Access**	**States**	**Reset Value**
15:0	Reserved	RO		00000000 00000000

24.16 Register 15 (0Fh) – 1000BASE-T Status Extension Register #1

Register 15 (0Fh) – 1000BASE-T Status Extension Register #1				
Bit	**Name**	**Access**	**States**	**Reset Value**
15	1000BASE-X FDX Capability	RO	1 = PHY is 1000BASE-X FDX capable 0 = PHY is not 1000BASE-X FDX capable	0
14	1000BASE-X HDX Capability	RO	1 = PHY is 1000BASE-X HDX capable 0 = PHY is not 1000BASE-X HDX capable	0
13	1000BASE-T FDX Capability	RO	1 = PHY is 1000BASE-T FDX capable 0 = PHY is not 1000BASE-T FDX capable	1
12	1000BASE-T HDX Capability	RO	1 = PHY is 1000BASE-T HDX capable 0 = PHY is not 1000BASE-T HDX capable	1
11:0	Reserved	RO		000000000000

24.17 Register 16 (10h) – 100BASE-TX Status Extension Register

Register 16 (10h) – 100BASE-TX Status Extension Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	100BASE-TX Descrambler Locked	RO	1 = Descrambler locked 0 = Descrambler not locked	0	
14	100BASE-TX Lock Error Detected	RO LH	1 = Lock error detected since last read 0 = Lock error not detected since last read	0	
13	100BASE-TX Disconnect State	RO LH	1 = PHY 100BASE-TX link disconnected 0 = PHY 100BASE-TX link not disconnected	0	
12	100BASE-TX Current Link Status	RO	1 = PHY 100BASE-TX link active 0 = PHY 100BASE-TX link inactive	0	
11	100BASE-TX Receive Error Detected	RO LH	1 = Receive error detected since last read 0 = Receive error not detected since last read	0	
10	100BASE-TX Transmit Error Detected	RO LH	1 = Transmit error detected since last read 0 = Transmit error not detected since last read	0	
9	100BASE-TX SSD (Start-of-Stream Delimiter) Error Detected	RO LH	1 = SSD error detected since last read 0 = SSD error not detected since last read	0	
8	100BASE-TX ESD (End-of-Stream Delimiter) Error Detected	RO LH	1 = ESD error detected since last read 0 = ESD error not detected since last read	0	
7:0	Reserved	RO		--	

24.18 Register 17 (11h) – 1000BASE-T Status Extension Register #2

Register 17 (11h) – 1000BASE-T Status Extension Register #2					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	1000BASE-T Descrambler Locked	RO	1 = Descrambler locked 0 = Descrambler not locked	0	
14	1000BASE-T Lock Error Detected	RO LH	1 = Lock error detected since last read 0 = Lock error not detected since last read	0	
13	1000BASE-T Disconnect State	RO LH	1 = PHY 1000BASE-T link disconnected 0 = PHY 1000BASE-T link not disconnected	0	
12	1000BASE-T Current Link Status	RO	1 = PHY 1000BASE-T link active 0 = PHY 1000BASE-T link inactive	0	
11	1000BASE-T Receive Error Detected	RO LH	1 = Receive error detected since last read 0 = Receive error not detected since last read	0	
10	1000BASE-T Transmit Error Detected	RO LH	1 = Transmit error detected since last read 0 = Transmit error not detected since last read	0	
9	1000BASE-T SSD (Start-of-Stream Delimiter) Error Detected	RO LH	1 = SSD error detected since last read 0 = SSD error not detected since last read	0	
8	1000BASE-T ESD (End-of-Stream Delimiter error) Error Detected	RO LH	1 = ESD error detected since last read 0 = ESD error not detected since last read	0	
7	1000BASE-T Carrier Extension Error Detected	RO LH	1 = Carrier extension error detected since last read 0 = Carrier extension error not detected since last read	0	
6	Non-compliant BCM5400 Detected	RO	1 = Non-compliant BCM5400 detected 0 = Non-compliant BCM5400 not detected	0	
5:0	Reserved	RO		--	

24.19 Register 18 (12h) – Bypass Control Register

Register 18 (12h) – Bypass Control Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Transmit Disable	R/W	1 = Transmitter disabled in PHY 0 = Transmitter enabled	0	
14:9	Reserved	RO		--	
8	1000BT Transmitter Test Clock Enable	R/W	1 = Enable TX_TCLK test output on $CLK125_{micro}$ pin 0 = Disable TX_TCLK test output on $CLK125_{micro}$ pin	0	
7:6	Reserved	RO		--	
5	Disable Automatic Pair Swap Correction	R/W	1 = Disable pair swap correction 0 = Enable pair swap correction	0	S
4	Disable Polarity Correction	R/W	1 = Disable polarity inversion correction 0 = Enable polarity inversion correction	0	S
3	Parallel-Detect Control	R/W	1 = Do not ignore advertised ability 0 = Ignore advertised ability	1	S
2	Reserved	RO		--	
1	Disable Automatic 1000BASE-T Next-Page Exchange	R/W	1 = Disable automatic 1000BASE-T Next-Page exchanges 0 = Enable automatic 1000BASE-T Next-Page exchanges	0	S
0	125MHz $_{MAC}$ Clock Output Enable	R/W	1 = Enable 125MHz output clock pin $CLK125_{MAC}$ 0 = Disable 125MHz output clock pin $CLK125_{MAC}$	1	S

18.15 – Transmit Disable

When bit 18.15 is set to “1”, the analog blocks are powered down and zeros are sent to the DAC.

decoder can by bypassed, receiving symbols through the 4-D slicer instead. In 100BASE-TX mode, to pass the unaligned symbols directly to the MII interface, this control bit should be set only when the 4B5B decoder is also bypassed.

18.8 – 1000BT Transmitter Test Clock Enable

When bit 18.8 is written to a “1”, the $CLK125_{micro}$ output pin becomes a test pin for the transmit clock “TX_TCLK” of a particular PHY port. This capability is intended to enable measurement of transmitter timing jitter, as specified in IEEE Standard 802.3-2002, section 40.6.1.2.5. When in IEEE-specified transmitter test modes 2 or 3 (see IEEE 802.3-2002, section 40.6.1.1.2 and MII Register bits 9.15:13), the peak-to-peak jitter of the zero-crossings of the differential signal output at the MDI, relative to the corresponding edge of TX_TCLK, is measured. The corresponding edge of TX_TCLK is the edge of the transmit test clock, in polarity and time, that generates the zero-crossing transition being measured.

While transmitter test mode clocks TX_TCLK_n are intended only for characterization test purposes, $CLK125_{micro}$ is intended, for example, to serve as a general purpose system or MAC reference clock.

Five distinct clock signals can be multiplexed onto the VSC8244’s $CLK125_{micro}$ pin, depending on a combination of the settings of MII Register bits 9.15:13, MII Register bit 18.8, and MII Register bit 18.0 (CLK125 Output Enable), as specified in the following table:

Table 37. Transmitter Test Clock Enable

Signal Multiplexed onto CLK125 Pin	Enabled by MII Register States
TX_TCLK_0	PHY0, ((9.15:13 == 010) || (9.15:13 == 011) || (18.8 ==1))
TX_TCLK_1	PHY1, ((9.15:13 == 010) || (9.15:13 == 011) || (18.8 ==1))
TX_TCLK_2	PHY2. ((9.15:13 == 010) || (9.15:13 == 011) || (18.8 ==1))
TX_TCLK_3	PHY3, ((9.15:13 == 010) || (9.15:13 == 011) || (18.8 ==1))
CLK125[1]	PHY0, 18.0 == 1

[1] Only PHY Port 0's bit 18.0 controls the operation of CLK125 (see Section 24.19: "Register 18 (12h) – Bypass Control Register").

18.5 – Disable Automatic Pair Swap Correction[1]

When bit 18.5 is set to "0", the PHY automatically corrects pair swaps between subchannels A and B, and between subchannels C and D, due to "MDI/MDI-X crossover". It will also correct pair swaps between subchannels C and D due to cabling errors. When bit 18.5 is set to "1", the PHY does not correct pair swaps.

18.4 – Disable Polarity Correction[1]

When bit 18.4 is set to "0", the PHY automatically corrects polarity inversion on all the subchannels. When bit 18.4 is set to "1", the PHY does not compensate for polarity inversions.

18.3 – Parallel-Detect Control

When bit 18.3 is "1", MII Register 4, bits [8:5], are taken into account when attempting to parallel-detect. This is the default behavior expected by the standard. Setting 18.3 to a "0" will result in Auto-Negotiation ignoring the advertised abilities, as specified in MII Register 4, during parallel detection of a non-auto-negotiating 10BASE-T or 100BASE-TX PHY.

18.2 – Disable Pulse Shaping Filter[1]

When bit 18.2 is set to "1", the 1000BASE-T two-tap digital transmit filter is disabled.

18.1 – Disable Automatic 1000BASE-T Next-Page Exchanges

Bit 18.1 is used to control the automatic exchange of 1000BASE-T Next-Pages defined in IEEE 802.3-2002 (Annex 40C). When this bit is set, the automatic exchange of these pages is disabled, and the control is returned to the user through the SMI after the base page has been exchanged. The user then has complete responsibility to:

- send the correct sequence of Next-Pages to the Link Partner, *and*
- determine common capabilities and force the device into the correct configuration following successful exchange of pages.

When bit 18.1 is reset to "0", the 1000BASE-T related Next-Pages are automatically exchanged without user intervention. If the Next Page bit 4.15 was set by the user in the Auto-Negotiation Advertisement register at the time the Auto-Negotiation was restarted, control is returned to the user for additional Next-Pages following the 1000BASE-T Next-Page exchange.

If both 18.1 and 4.15 are reset when an Auto-Negotiation sequence is initiated, all Next-Page exchange is automatic, including sourcing of null pages. No user notification is provided until either Auto-Negotiation completes or fails. See the description of Register bit 4.15 for more details on standard Next-Page exchanges.

[1]This bit applies only in 1000BASE-T mode

18.0 – Enable 125MHz MAC Free-Running Clock Output

When bit 18.0 is set to “1”, the VSC8244 provides a free-running, general-purpose 125MHz clock on the $CLK125_{MAC}$ output pin. The electrical specifications for this clock corresponds to the current setting for $VDDIO_{MAC}$. This clock can be used by a MAC, a switch, or other synchronous logic. By default, this pin is enabled, which enables the clock output, independent of the status of any link, unless a hardware reset is active (which also powers down the PLL). When disabled, this pin is normally driven low. Note that only PHY Port 0’s bit 18.0 controls the operation of $CLK125_{MAC}$.

24.20 Register 19 (13h) – Reserved

Register 19 (13h) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		--	

24.21 Register 20 (14h) – Reserved

Register 20 (14h) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		--	

24.22 Register 21 (15h) – Reserved

Register 21 (15h) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		--	

24.23 Register 22 (16h) – Extended Control & Status Register

	Register 22 (16h) – Extended Control & Status Register				
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Force 10BT Link High	R/W	1 = Disable link integrity test 0 = Enable link integrity test	0	S
14	Jabber Detect Disable	R/W	1 = Disable jabber detect 0 = Enable jabber detect	0	S
13	Disable 10BASE-T echo	R/W	1 = Disable 10BASE-T echo 0 = Enable 10BASE-T echo	1	S
12	Reserved	RO	-	--	
11:10	10BASE-T Squelch Control	R/W	00 = Normal squelch 01 = Low squelch 10 = High squelch 11 = Reserved	00	S
9	Sticky Reset Enable	R/W	1 = All bits marked as sticky will retain their values during software reset 0 = All bits marked as sticky will be changed to default values during software reset	1	SS
8	EOF Error Detected	RO SC	1 = EOF error detected since last read 0 = EOF error not detected since last read	0	
7	10BASE-T Disconnect State	RO SC	1 = 10BASE-T link disconnected 0 = 10BASE-T link connected	0	
6	10BASE-T Link Status	RO	1 = 10BASE-T link active 0 = 10BASE-T link inactive	0	
5:0	Reserved	RO	-	--	

22.15 – Force 10BT Link High

When bit 22.15 is set to “0”, the VSC8244 link integrity state machine runs automatically; it also controls link pass status. When bit 22.15 is set to “1”, the link integrity state machine is bypassed, and the PHY is forced into link pass status.

22.14 – Disable Jabber Detect

When bit 22.14 is set to “0”, the VSC8244 automatically shuts off the transmitter when a transmission request exceeds the IEEE-specified time limit. When bit 22.14 is set to “1”, transmission requests are allowed to be arbitrarily long without shutting down the transmitter.

22.13 – Disable 10BASE-T Echo Mode

When bit 22.13 is set to “1”, the logical state of the TX_EN pin will not echo onto the CRS pin, effectively disabling CRS from being asserted in half-duplex operation. When bit 22.13 is set to “0”, the TX_EN pin will be echoed onto the CRS pin. Data on TXD is echoed to RXD in 10BASE-T mode only.

22.11:10 – Squelch Control

When bits 22.11:10 are set to “00”, the VSC8244 uses the squelch threshold levels prescribed by the IEEE’s 10BASE-T specification. When bits 22.11:10 are set to “01”, the squelch level is decreased, which may improve the bit error rate performance on long loops. When bits 22.11:10 are set to “10”, the squelch level is increased, which may improve the bit error rate in high-noise environments.

22.9 - Sticky Reset Enable

When bit 22.9 is set, all MII register bits that are marked with an “S” in the “sticky” column will retain their values during a software reset. When cleared, all MII register bits that are marked with an “S” in the “sticky” column will be changed to their default values during a software reset. Note that bits marked with an “SS” retain their values across software reset regardless of the setting of bit 22.9.

22.8 – EOF Error

When bit 22.8 returns a “1”, a defective EOF (End-of-Frame) sequence has been received since the last time this bit was read. This bit is automatically set to “0” when it is read.

22.7 – 10BASE-T Disconnect State

Bit 22.7 is set to “1” if the 10BASE-T connection has been broken by the carrier integrity monitor since the last read of this bit; otherwise, this bit is set to “0”.

24.24 Register 23 (17h) – Extended PHY Control Register #1

	Register 23 (17h) – Extended PHY Control Register #1				
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Reserved	RO	Always set to 0	--	
14:12	MAC/Media Interface Mode Select	R/W	See table in register description below	CMODE	SS
11:10	RGMII TX_CLK Skew Selection	R/W	00 = No skew on TX_CLK 01 = 1.5ns skew on TX_CLK 10 = 2ns skew on TX_CLK 11 = 2.5ns skew on TX_CLK	CMODE	S
9:8	RGMII RX_CLK Skew Selection	R/W	00 = No skew on RX_CLK 01 = 1.5ns skew on RX_CLK 10 = 2ns skew on RX_CLK 11 = 2.5ns skew on RX_CLK	CMODE	S
7:6	Reserved	RO	-	--	
5	RX Idle Clock Enable	R/W	1 = 25MHz clock on RX_CLK pin enabled in Act-iPHY mode 0 = 25MHz clock on RX_CLK pin disabled in Act-iPHY mode	1	SS
4	Reserved	RO		--	
3	Far End Loopback Mode Enable	R/W	1 = Far end loopback is enabled 0 = Far end loopback is disabled	0	
2:1	MAC/Media Interface Mode Select	R/W	See table in register description below	CMODE	SS
0	EEPROM Status	RO	1 = EEPROM is detected on EEPROM interface 0 = EEPROM is not detected on EEPROM interface	0	

23.14:12, 2:1– MAC/Media Interface Mode Select

Bits 23.14:12 and 23.2:1 are used to select the MAC interface modes and the media interface modes.

IMPORTANT: To change operating modes, write bits 14:12 and 2:1 to their intended settings. Write a 1 to register bit 0:15 for the change to take effect. This sequence should be completed first, before all other configuration writes to other registers are perfomed.

The reset value for these bits is dependent upon the state of the MAC Interface bits in the CMODE hardware configuration. All combinations of these bits not indicated below are reserved:

Table 38. MAC/Media Interface Mode Select

Bits 23.14:12	Bits 23.2:1	CMODE MAC Interface [2:1]	MAC Interface	Media Interface	Options
001	10	11	RGMII	CAT-5	
101	00	-	RTBI	CAT-5	Clause 37 autonegotiation disabled
100	01	00	RTBI	CAT-5	Clause 37 autonegotiation enabled
100	10	-	RTBI	CAT-5	Clause 37 autonegotiation enabled - media converter
100	11	-	RTBI	CAT-5	Clause 37 autonegotiation enabled - interlock disabled
100	00	-	RTBI	CAT-5	Clause 37 autonegotiation autosense

23.11:10 – RGMII TX_CLK Skew Selection

Bits 23.11:10 specify the amount of clock delay added to the TX_CLK line inside the VSC8244 in RGMII and RTBI interfaces. By enabling this internal delay, a PCB “trombone” delay is not required as specified by the RGMII standard. Multiple values are provided to compensate for PCB trace skews. The default values of these bits are specified by the RGMII Skew bits in the CMODE hardware configuration.

23.9:8 – RGMII RX_CLK Skew Selection

Bits 23.9:8 specify the amount of clock delay added to the RX_CLK line inside the VSC8244 in RGMII and RTBI interfaces. By enabling this internal delay, a PCB “trombone” delay is not required as specified by the RGMII standard. Multiple values are provided to compensate for PCB trace skews. The default values of these bits are specified by the RGMII Skew bits in the CMODE hardware configuration.

23.5 – RX Idle Clock Enable

When bit 23.5 is set to “1”, a 25MHz clock is enabled on the RX_CLK pin when the VSC8244 is in ActiPHY mode. When bit 23.5 is cleared, the RX_CLK pin remains low during ActiPHY mode. This clock is enabled by default.

23.3 – Far End Loopback Mode Enable

When bit 23.3 is set to “1”, all incoming data from the link partner on the current media interface is retransmitted back to the link partner on the media interface. In addition the incoming data will also appear on the RX pins of the MAC interface. Any data present on the TX pins of the MAC interface is ignored by the VSC8244 when bit 23.3 is set. In order to avoid loss of data, bit 23.3 should not be set while the VSC8244 is receiving data on the media interface. Bit 23.3 applies to all MAC interfaces and to all media interfaces in the VSC8244. When bit 23.3 is cleared, the VSC8244 resumes normal operation. This bit is cleared by default.

23.0 – EEPROM Status

When bit 23.0 is set to “1”, an EEPROM has been detected on the external EEPROM interface. When cleared, bit 23.0 indicates that no EEPROM has been detected.

24.25 Register 24 (18h) – Extended PHY Control Register #2

Register 24 (18h) – Extended PHY Control Register #2					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:13	100/1000BASE-T Edge Rate Control	R/W	011 = +3 edge rate (slowest) 010 = +2 edge rate 001 = +1 edge rate 000 = Nominal edge rate 111 = -1 edge rate 110 = -2 edge rate 101 = -3 edge rate 100 = -4 edge rate (fastest)	000	S
12	Enable PICMG Reduced Power Mode	R/W	1 = PICMG reduced power mode is enabled 0 = PICMG reduced power mode is disabled	0	S
11:10	Reserved	RO	-	--	
9:7	1000BT TX FIFO Depth Control for RGMII	R/W	000 = 5 symbols 001 = 4 symbols 010 = 3 symbols 011 = 2 symbols 100 = 1 symbol 101 to 111 = Reserved	100	S
6:4	1000BT RX FIFO Depth Control for RTBI	R/W	000 = 5 symbols 001 = 4 symbols 010 = 3 symbols 011 = 2 symbols 100 = 1 symbol 101 to 111 = Reserved	100	S
3:1	Reserved	RO	-	--	
0	1000BT Connector Loopback	R/W	1 = Active (see Section 21.5: "Connector Loopback" for more information) 0 = Disabled	0	

24.15:13 – 100/1000BASE-T Edge Rate Control

Bits 24.15:13 control the transmit DAC slew rate in 100BASE-TX and 1000BASE-T modes only, as shown above. The difference between each setting is approximately 200ps to 300ps, with the “+3” setting resulting in the slowest edge rate, and the “-4” setting resulting in the fastest edge rate.

24.12 - Enable PICMG Reduced Power Mode

Setting bit 24.12 turns off some portions of the PHY's DSP block and reduces the PHY's Operating power. The DSP performance characteristics in this mode are configured to support the channel characteristics specified in the PICMG 2.16 and PICMG 3.0 specifications. See www.picmg.org for more information. This bit can be set in order to reduce power consumption in applications where the signal to noise ratio on the media is high, such as ethernet over the backplane, or where the cable length is short (<10m). PICMG reduced power mode may be used in certain applications with capacitively coupled media, rather than transformer coupled, to reduce PCB area and cost. Refer to Vitesse Application Note: Transformerless Ethernet Concept and Applications for more information.

24.9:7 – 1000BT TX FIFO Depth Control for RGMII

Bits 24.9:7 control symbol buffering for the transmit synchronization FIFO used in all 1000BT modes. An internal FIFO is used to synchronize the clock domains between the MAC transmit clock and the PHY's clock (e.g., REFCLK), used to transmit symbols on the local PHY's twisted pair interface.

The IEEE mode supports up to 1518-byte packet size with the minimum inter-packet gap (IPG). The jumbo packet mode adds latency to the path to support up to 9600-byte packets with the minimum inter-packet gap (IPG). When using jumbo packet mode, a larger IPG is recommended due to the possible compression of the IPG at the output of the FIFO.

24.6:4 – 1000BT RX FIFO Depth Control for RTBI

Used in 1000BT RTBI modes only, bits 24.6:4 control symbol buffering as determined by the receive synchronization FIFO. An internal FIFO is used to synchronize the clock domains between the MAC receive clock and the PHY's clock (e.g., REFCLK), used to receive symbols on the local PHY's twisted pair interface.

The IEEE mode supports up to 1518-byte packet size with the minimum inter-packet gap (IPG). The jumbo packet mode adds latency to the path to support up to 9600-byte packets with the minimum inter-packet gap (IPG). When using jumbo packet mode, a larger IPG is recommended due to the possible compression of the IPG at the output of the FIFO.

24.26 Register 25 (19h) – Interrupt Mask Register

Register 25 (19h) – Interrupt Mask Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Interrupt Pin Enable	R/W	1 = Enable interrupt pin 0 = Disable interrupt pin	0	S
14	Speed State-Change Interrupt Mask	R/W	1 = Enable Speed interrupt 0 = Disable Speed interrupt	0	S
13	Link State-Change/ Energy Detect Interrupt Mask	R/W	1 = Enable Link State/ Energy Detect interrupt 0 = Disable Link State/ Energy Detect interrupt	0	S
12	FDX State-Change Interrupt Mask	R/W	1 = Enable FDX interrupt 0 = Disable FDX interrupt	0	S
11	Auto-Negotiation Error Interrupt Mask	R/W	1 = Enable Auto-Negotiation Error interrupt 0 = Disable Auto-Negotiation Error interrupt	0	S
10	Auto-Negotiation-Done/ Interlock Done Interrupt Mask	R/W	1 = Enable Auto-Negotiation-Done/ Interlock Done interrupt 0 = Disable Auto-Negotiation-Done/ Interlock Done interrupt	0	S
9	In-line Powered Device Detected Interrupt Mask	R/W	1 = Enable In-line Powered Device Detected interrupt 0 = Disable In-line Powered Device Detected interrupt	0	S
8	Symbol Error Interrupt Mask	R/W	1 = Enable Symbol Error interrupt 0 = Disable Symbol Error interrupt	0	S
7	Descrambler Lock-Lost Interrupt Mask	R/W	1 = Enable Lock-Lost interrupt 0 = Disable Lock-Lost interrupt	0	S
6	TX FIFO Interrupt Mask	R/W	1 = Enable TX FIFO interrupt 0 = Disable TX FIFO interrupt	0	S
5	RX FIFO Interrupt Mask	R/W	1 = Enable RX FIFO interrupt 0 = Disable RX FIFO interrupt	0	S
4	Reserved	RO	-	--	
3	False Carrier Interrupt Mask	R/W	1 = Enable False Carrier interrupt 0 = Disable False Carrier interrupt	0	S
2	Cable Impairment Detect Interrupt Mask	R/W	1 = Enable Cable Impairment Detect interrupt 0 = Disable Cable Impairment Detect interrupt	0	S
1	MASTER/SLAVE Interrupt Mask	R/W	1 = Enable MASTER/SLAVE interrupt 0 = Disable MASTER/SLAVE interrupt	0	S
0	RX_ER Interrupt	R/W	1 = Enable RX_ER interrupt 0 = Disable RX_ER interrupt	0	S

25.15 – Interrupt Pin Enable

When bit 25.15 is set to “1”, the hardware interrupt is enabled, meaning that the state of the external interrupt pin (MDINT_n) can be influenced by the state of the Interrupt Status bit (26.15). When bit 25.15 is set to “0”, the interrupt status bits (Register 26) continue to be set in response to interrupts, but the interrupt hardware pin MDINT_n on the VSC8244 will not be influenced by this particular PHY.

24.27 Register 26 (1Ah) – Interrupt Status Register

Register 26 (1Ah) – Interrupt Status Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Interrupt Status	RO SC	1 = Interrupt pending 0 = No interrupt pending	0	
14	Speed State-Change Interrupt Status	RO SC	1 = Speed interrupt pending	0	
13	Link State-Change/ Energy Detect Interrupt Status	RO SC	1 = Link State-Change/ Energy Detect interrupt pending	0	
12	FDX State-Change Interrupt Status[1]	RO SC	1 = FDX interrupt pending	0	
11	Auto-Negotiation Error Interrupt Status	RO SC	1 = Auto-Negotiation Error interrupt pending	0	
10	Auto-Negotiation-Done/ Interlock Done Interrupt Status	RO SC	1 = Auto-Negotiation-Done/ Interlock Done interrupt pending	0	
9	In-line Powered Device Interrupt Status	RO SC	1 = In-line Powered Device interrupt pending	0	
8	Symbol Error Interrupt Status	RO SC	1 = Symbol Error interrupt pending	0	
7	Descrambler Lock-Lost Interrupt Status	RO SC	1 = Lock-Lost interrupt pending	0	
6	TX FIFO Interrupt Status	RO SC	1 = TX FIFO interrupt pending	0	
5	RX FIFO Interrupt Status	RO SC	1 = RX FIFO interrupt pending	0	
4	Reserved	RO	-	--	
3	False Carrier Interrupt Status	RO SC	1 = False Carrier interrupt pending	0	
2	Cable Impairment Detect Interrupt Status	RO SC	1 = Cable Impairment Detect interrupt pending	0	
1	MASTER/SLAVE Interrupt Status	RO SC	1 = MASTER/SLAVE Error interrupt pending	0	
0	RX_ER Interrupt Status	RO	1 = RX_ER interrupt pending 0 = No RX_ER interrupt pending	0	

26.15 – Interrupt Status

When bit 26.15 is set to “1”, an unacknowledged interrupt is pending. The cause of the interrupt can be determined by reading the interrupt status bits in this register. This bit is automatically cleared when read.

26.14 – Speed State-Change Interrupt Status

When the operating speed of the PHY changes, bit 26.14 is set to "1" if bit 26.14 is set to "1" and if bit 0.12 is also set to "1". This bit is automatically cleared when read.

26.13 – Link State-Change/ Energy Detect Interrupt Status

When the link status of the PHY changes, or if ActiPHY mode is enabled, and energy is detected on the media, bit 26.13 is set to “1” if bit 25.13 is also set to “1”. This bit is automatically cleared when read.

26.12 – FDX State-Change Interrupt Status

When the FDX/HDX status of the PHY changes, bit 26.12 is set to "1" if bit 26.12 is set to "1" and if bit 0.12 is also set to "1". This bit is automatically cleared when read.

26.11 – Auto-Negotiation Error Interrupt Status

When an error is detected by the Auto-Negotiation state machine, bit 26.11 is set to “1” if bit 25.11 is also set to “1”. This bit is automatically cleared when read.

26.10 – Auto-Negotiation-Done/Interlock Done Interrupt Status

When the Auto-Negotiation state machine finishes a negotiation process, bit 26.10 is set to “1” if bit 25.10 is also set to “1”. This bit is automatically cleared when read.

26.9 – In-line Powered Device Interrupt Status

When a device requiring in-line power over CAT-5 is detected, bit 26.9 is set to “1” if bit 25.9 is also set to “1”. This bit is automatically cleared when read.

26.8 – Symbol Error Interrupt Status

When a symbol error is detected by the descrambler, bit 26.8 is set to “1” if bit 25.8 is also set to “1”. This bit is automatically cleared when read.

26.7 – Descrambler Lock-Lost Interrupt Status

When the descrambler loses lock, bit 26.7 is set to “1” if bit 25.7 is also set to “1”. This bit is automatically cleared when read.

26.6 – TX FIFO Interrupt Status

When the TX FIFO enters an underflow or overflow condition, bit 26.6 is set to “1” if bit 25.6 is also set to “1”. This bit is automatically cleared when read.

26.5 – RX FIFO Interrupt Status

When the RX FIFO enters an underflow or overflow condition, bit 26.5 is set to “1” if bit 25.5 is also set to “1”. This bit is automatically cleared when read.

26.3 – False Carrier Detect Interrupt Status

When the PHY has detected a false carrier, bit 26.3 is set to “1” if bit 25.3 is also set to “1”. This bit is automatically cleared when read,

26.2 – Cable Impairment Detect Interrupt Status

When the PHY has detected an impairment on the CAT-5 media, bit 26.3 is set to “1” if bit 25.3 is also set to “1”. This bit is automatically cleared when read. This feature is disabled if MII register bits 4:8.5 are all set to "0".

26.1 – MASTER/SLAVE Resolution Error Interrupt Status

When a MASTER/SLAVE resolution error is detected, bit 26.1 is set to “1” if bit 25.1 is also set to “1”. This bit is automatically cleared when read.

26.0 – RX_ER Interrupt Status

When an RX_ER condition occurs, bit 26.0 is set to “1”. This bit is automatically cleared when read.

24.28 Register 27 (1Bh) – LED Control Register

Register 27 (1Bh) – LED Control Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:14	LED Pin 4 Configuration	R/W	00 = Duplex/Collision 01 = Activity 10 = Link Fault 11 = Link/Activity	CMODE	S
13:12	LED Pin 3 Configuration	R/W	00 = Collision 01 = Duplex/Collision 10 = Reserved 11 = Rx	CMODE	S
11:10	LED Pin 2 Configuration	R/W	00 = Link10/Activity 01 = Duplex/Collision 10 = Link/Activity 11 = Tx	CMODE	S
9:8	LED Pin 1 Configuration	R/W	00 = Link100/Activity 01 = Link10/100/Activity 10 = Link/Activity 11 = Link100/1000/Activity	CMODE	S
7:6	LED Pin 0 Configuration	R/W	00 = Link1000/Activity 01 = Link/Activity w/ Serial output on LED pins 1 and 2 10 = Fault 11 = Rx	CMODE	S
5	LED Pulse-stretch Rate/ Blink Rate	R/W	1 = 10Hz blink rate/ 100ms pulse-stretch 0 = 5Hz blink rate/ 200ms pulse-stretch	0	S
4	LED Pulsing Enable	R/W	1 = Enable 5KHz, 20% duty cycle LED pulsing for power savings 0 = LED pulsing disabled	0	S
3	LED Pulse-Stretch/ Blink Select	R/W	1 = Collision, Activity, Rx and Tx functions will pulse-stretch when active. 0 = Collision, Activity, Rx and Tx functions will blink when active.	CMODE	S
2	LED Link/Activity Behavior	R/W	1 = Link function indicates link status only 0 = Link function will blink or flash when activity is present. Blink/flash behavior is selected by Pulse-Stretch Enable and Blink/Pulse-Stretch Rate bits.	CMODE	S
1	LED Link10/100/1000/Activity Behavior	R/W	1 = Link10, Link 100, Link1000, Link10/100, and Link100/1000 LEDs indicates link status only 0 = Link10, Link 100, Link1000, Link10/100, and Link100/1000 LEDs will blink or flash when activity is present. Blink/flash behavior is selected by Pulse-Stretch Enable and Blink/ Pulse-Stretch Rate bits.	CMODE	S
0	LED Duplex/Collision Behavior	R/W	1 = Duplex function indicates duplex status only 0 = Duplex function will blink or flash when collision is present	CMODE	S

27.15:6 – LED Pin Configuration

Each of the five LED pins on each port of the VSC8244 can be configured for one of four functions. These functions are different for each LED pin. Bits 27.15:6 are used to select the function for each LED pin. The reset value of these bits is set by the LED configuration bits in the CMODE hardware configuration. NOTE: if bits 27.7:6=01, then LED1 and LED2 become serial outputs.

24.29 Register 28 (1Ch) – Auxiliary Control & Status Register

Register 28 (1Ch) – Auxiliary Control & Status Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Auto-Negotiation Complete	RO	1 = Auto-Negotiation complete 0 = Auto-Negotiation not complete	0	
14	Auto-Negotiation Disabled	RO	1 = Auto-Negotiation was disabled 0 = Auto-Negotiation is enabled	0	
13	MDI/MDI-X Crossover Indication	RO	1 = MDI/MDI-X crossover detected 0 = MDI/MDI-X crossover not detected	0	
12	CD Pair Swap	RO	1 = CD pairs are swapped 0 = CD pairs are not swapped	0	
11	A Polarity Inversion	RO	1 = Polarity swapped on pair A 0 = Polarity not swapped on pair A	0	
10	B Polarity Inversion	RO	1 = Polarity swapped on pair B 0 = Polarity not swapped on pair B	0	
9	C Polarity Inversion	RO	1 = Polarity swapped on pair C 0 = Polarity not swapped on pair C	0	
8	D Polarity Inversion	RO	1 = Polarity swapped on pair D 0 = Polarity not swapped on pair D	0	
7	Reserved	RO	-	--	
6	ActiPHY Mode Enable	R/W	1 = Enable ActiPHY power management 0 = Disable ActiPHY power management	CMODE	S
5	FDX Status	RO	1 = Full Duplex 0 = Half Duplex	0	
4:3	Speed Status	RO	00 = Speed is 10BASE-T 01 = Speed is 100BASE-TX 10 = Speed is 1000BASE-T 11 = Reserved	00	
2	Reserved	RO	-	--	
1:0	ActiPHYTM Sleep Timer	R/W	00 = 1 Second 01 = 2 Seconds 10 = 3 Seconds 11 = 4 Seconds	01	

28.15 – Auto-Negotiation Complete

This bit is a copy of bit 1.5, duplicated here for convenience.

28.14 – Auto-Negotiation Disabled

When bit 28.14 is read as a “1”, this bit indicates that the Auto-Negotiation process has been disabled. This happens only when register bit 0.12 is set to “0”.

28.13 – MDI/MDI-X Crossover Indication

When bit 28.13 returns a “1”, the Auto-Negotiation state machine has determined that crossover does not exist in the signal path. The crossover will therefore be performed internally to the PHY, as described by the MDI/MDI-X crossover specification.[1]

[1]This bit is valid only after descrambler lock has been achieved and as long as bit 18.5 is set to “0”.

28.12 – CD Pair Swap[1]

When bit 28.12 returns a “1”, the PHY has determined that subchannel cable pairs C and D have been swapped between the far-end transmitted and the receiver. When bit 28.12 returns a “1”, the PHY internally swaps pairs C and D (as long as bit 18.5 is set to “0”).[1]

28.11 – A Polarity Inversion

When bit 28.11 returns a “1”, the PHY has determined that the polarity of subchannel cable pair A has been inverted between the far-end transmitter and the near-end receiver. When bit 28.11 returns a “1”, the PHY internally corrects the pair inversion. Polarity-inversion correction runs in all three modes; as a result, the state of 28.11 is valid only when bit 1.5 is set to “1”.

28.10 – B Polarity Inversion

When bit 28.10 returns a “1”, the PHY has determined that the polarity of subchannel cable pair B has been inverted between the far-end transmitter and the near-end receiver. When bit 28.10 returns a “1”, the PHY internally corrects the pair inversion. Polarity-inversion correction runs in all three modes; as a result, the state of 28.10 is valid only when bit 1.5 is set to “1”.

28.9 – C Polarity Inversion[2]

When bit 28.9 returns a “1”, the PHY has determined that the polarity of subchannel cable pair C has been inverted between the far-end transmitter and the near-end receiver. When bit 28.9 returns a “1”, the PHY internally corrects the pair inversion. Polarity-inversion correction runs in all three modes; as a result, the state of 28.9 is valid only when bit 1.5 is set to “1”.

28.8 – D Polarity Inversion[1]

When bit 28.8 returns a “1”, the PHY has determined that the polarity of subchannel cable pair D has been inverted between the far-end transmitter and the near-end receiver. When bit 28.8 returns a “1”, the PHY internally corrects the pair inversion. Polarity-inversion correction runs in all three modes; as a result, the state of 28.8 is valid only when bit 1.5 is set to “1”.

28.6 - Enable ActiPHY Mode

When bit 28.6 is set to a “1”, the ActiPHY power management mode is set in the VSC8244. The reset value for this bit is determined by the ActiPHY bit in the CMODE hardware configuration.

28.5 – FDX Status

Bit 28.5 indicates the actual FDX/HDX operating mode of the PHY.

28.4:3 – Speed Status

Bits 27.4:3 indicate the actual operating speed of the PHY.

28.1:0 – ActiPHY™ and AMS Sleep Timer

This sets the time period the PHY stays in ‘Low Power’ state when ActiPHY mode (MII Register Bit 28.6) is enabled before entering into the ‘LP Wake-up’ state. Refer to Section 19: "ActiPHY Power Management" for more information.

[1]This bit applies only in 1000BASE-T mode.

[2]This bit applies only in 1000BASE-T mode.

24.30 Register 29 (1Dh) – Reserved

Register 29 (1Dh) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO		--	

24.31 Register 30 (1Eh) - Reserved

Register 30 (1Eh) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO	-	--	

24.32 Register 31 (1Fh) – Extended Page Access

Register 31 (1Fh) – Extended Page Access					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:1	Reserved	RO	-	--	
0	Extended Page Access	WO	1 = MII registers 16:30 will access extended register set 0 = MII registers 16:30 will access standard register set	0	

31.0 - Extended Page Access

In order to provide additional functionality beyond the IEEE802.3 specified 32 MII registers, the VSC8244 contains an extended register set which supports an additional 15 registers. When bit 31.0 is set to a “1”, MII registers 16:30 will access the extended set of registers. The state of bit 31.0 has no effect on MII registers 0:15. This bit is write only and cannot be read back.

24.33 Register 16E (10h) - Reserved

Register 16E (10h) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:3	Reserved	RO	-	--	

24.34 Register 17E (11h) - CLK125$_{micro}$ Clock Enable

Register 17E (11h) – CLK125$_{micro}$ Clock Enable					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:1	Reserved	RO	-	--	
0	CLK125$_{micro}$ Clock Output Enable	R/W	1 = Enable CLK125$_{micro}$ output clock pin 0 = Disable CLK125$_{micro}$ output clock pin	0	S

17E.0 - Enable 125MHz$_{micro}$ Free-Running Clock Output

When this bit is set to “1”, the VSC8244 provides a free-running, general-purpose clock on the CLK125$_{micro}$ output pin. The electrical specifications for this clock corresponds to the current setting for VDDIO$_{micro}$. This clock can be used by a system manager CPU or other control logic. Please refer to MII Register 20E.8 to set the CLK125$_{micro}$ frequency. By default, this pin is disabled and must be set to a “1” in order to output a signal. When disabled, this pin is normally driven low. Note that only PHY Port 0’s bit 17E.0 controls the operation of CLK125$_{micro}$.

24.35 Register 18E (12h) - Reserved

Register 18E (12h) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO	-	--	

24.36 Register 19E (13h) - Reserved

Register 19E (13h) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO	-	--	

24.37 Register 20E (14h) - Extended PHY Control Register #3

Register 20E (14h) – Extended PHY Control Register #3					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:9	Reserved	RO	-	--	
8	$CLK125_{micro}$ Frequency	R/W	1 = 125MHz clock output on $CLK125_{micro}$ 0 = 4MHz clock output on $CLK125_{micro}$	0	S
7:5	Reserved	RO	-	--	
4	Enable Link Speed Auto-Downshift	R/W	1 = Enable auto link speed downshift 0 = Disable auto link speed downshift	CMODE	S
3:2	Link Speed Auto-Downshift Control	R/W	00 = Downshift after 2 failed attempts 01 = Downshift after 3 failed attempts 10 = Downshift after 4 failed attempts 11 = Downshift after 5 failed attempts	01	S
1	Link Speed Auto-Downshift Status	RO	0 = No downshift 1 = Downshift is required or has occurred	0	
0	Reserved	RO	-	--	

20E.8 - Clock Frequency Mode

The freqency of the $CLK125_{micro}$ pin can be changed by using bit 20E.8. This bit is only valid in PHY0.

20E.4 - Enable Link Speed Auto-Downshift

When bit 20E.4 is set to a “1”, the VSC8244 will “downshift” the autonegotiation advertisement to 100BASE-TX after the number of failed 1000BASE-T autonegotiation attempts specified in bits 20E.3:2. The reset value of this bit is determined by the Link Speed Downshift bit in the CMODE hardware configuration.

20E.3:2 - Link Speed Auto-Downshift Control

Bits 20E.3:2 determine the number of unsuccessful 1000BASE-T autonegotiation attempts that are required before the autonegotiation advertisement is “downshifted” to 100BASE-TX. These bits are valid only if bit 20E.4 is set.

20E.1 - Link Speed Auto-Downshift Status

When bit 20E.1 is set to a “1” and bit 20E.4 is set to a “1”, the current link speed is the result of a “downshift” to 100BASE-TX. When bit 20E.1 is set to a “1” and bit 20E.4 is cleared, the current link requires a “downshift” in order to be established.

24.38 Register 21E (15h) - EEPROM Interface Status and Control Register

Register 21E (15h) - EEPROM Interface Status and Control Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	Reserved	RO	-	--	
14	Re-read EEPROM on Software Reset	R/W	1 = Contents of EEPROM should be re-read on software reset 0 = Contents of EEPROM should not be re-read on software reset	0	SS
13	EEPROM Access Enable	R/W SC	1 = Execute read or write to EEPROM	0	
12	EEPROM Read/Write	R/W	1 = Read from EEPROM 0 = Write to EEPROM	1	
11	EEPROM Ready	RO	1 = EEPROM is ready for read/write 0 = EEPROM is busy	1	
10:0	EEPROM Address	R/W	EEPROM address to read/write	0	

21E.14 - Re-Read EEPROM on Software Reset

When bit 21E.14 is set to a “1”, the contents of the EEPROM will be re-read and reloaded into the MII registers upon software reset.

21E.13 - EEPROM Access Enable

When bit 21E.13 is set to a “1”, the EEPROM address in bits 21E.10:0 is written to or read from, based on the state of bit 21E.12. The data to read/write resides in register 22E.

21E.12 - EEPROM Read/Write

When bit 21E.12 is set to a “1”, the VSC8244 will read from the EEPROM when bit 21E.13 is set. When bit 21E.12 is cleared, the VSC8244 will write to the EEPROM when bit 21E.13 is set.

21E.11 - EEPROM Ready

When the VSC8244 is busy reading/writing to the EEPROM, bit 21E.11 will be cleared. Bit 21E.13 should not be set while bit 21E.11 is cleared.

21E.10:1 - EEPROM Address

These bits contain the EEPROM address that the VSC8244 will read from or write to when bit 21E.13 is set.

24.39 Register 22E (16h) - EEPROM Data Read/Write Register

Register 22E (16h) - EEPROM Data Read/Write Register					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:8	EEPROM Read Data	RO	8-bit data read from EEPROM	0	
7:0	EEPROM Write Data	R/W	8-bit data to write to EEPROM	0	

22E.15:18 - EEPROM Read Data

After an EEPROM read has occurred by setting bits 21E.13 and 21E.12 to a “1”, the data read from the EEPROM is placed in these bits.

22E.7:0 - EEPROM Write Data

When an EEPROM write is initiated by setting bits 21E.13 to a “1” and clearing bit 21E.12, the data from these bits is written to the EEPROM.

24.40 Register 23E (17h) - Extended PHY Control Register #4

Register 23E (17h) - Extended PHY Control Register #4					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:11	PHY Address	RO	PHY address latched on reset	CMODE	
10	Enable In-line Powered Device Detection	R/W	1 = In-line powered device detection is enabled 0 = In-line powered device detection is disabled	0	S
9:8	In-line Powered Device Detection Status	RO	00 = Searching for devices 01 = Device found which requires in-line power 10 = Device found which does not require in-line power 11 = Reserved	0	
7:0	CRC Counter	RO SC	CRC counter for Ethernet packet generator	0	

23E.15:11 - PHY Address

These bits contain the PHY address of the current PHY port. The reset value of these bits is determined by the PHY Address bits in the CMODE hardware configuration.

23E.10 - Enable In-line Powered Device Detection

When bit 23E.10 = 1, the VSC8244 will search for devices requiring CAT-5 in-line power as part of the autonegotiation process.

23E.9:8 - In-line Powered Device Detection Status

Bits 23E.9:8 are used by the station manager to determine if a device is connected to the VSC8244 which requires in-line power. These bits are only valid if bit 23E.10 = 1.

23E.7:0 - 1000BT CRC Counter

In 1000BT mode, these bits count the number of packets received that contain a CRC error. This counter will saturate at 0FFh and is cleared when read.

24.41 Register 24E (18h) – Reserved

Register 24E (18h) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO	-	--	

24.42 Register 25E (19h) – Reserved

Register 25E (19h) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO	-	--	

24.43 Register 26E (1Ah) – Reserved

Register 26E (1Ah) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO	-	--	

24.44 Register 27E (1Bh) – Reserved

Register 27E (1Bh) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO	-	--	

24.45 Register 28E (1Ch) – Reserved

Register 28E (1Ch) – Reserved					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15:0	Reserved	RO	-	--	

24.46 Register 29E (1Dh) - 1000BASE-T Ethernet Packet Generator (EPG) Register #1

Register 29E (1Dh) - 1000BASE-T Ethernet Packet Generator (EPG) Register #1					
Bit	**Name**	**Access**	**States**	**Reset Value**	**Sticky**
15	EPG Enable	R/W	1 = Enable EPG 0 = Disable EPG	0	
14	EPG Run/Stop	R/W	1 = Run EPG 0 = Stop EPG	0	
13	Transmission Duration	R/W	1 = Continuous 0 = Send 30,000,000 packets and stop	0	
12:11	Packet Length	R/W	00 = 125 bytes 01 = 64 bytes 10 = 1518 bytes 11 = 10,000 bytes (jumbo packet)	0	
10	Inter-packet Gap	R/W	1 = 8,192 ns 0 = 96 ns	0	
9:6	Destination Address	R/W	MSB's lower nibble of the 6-byte destination address	0001	
5:2	Source Address	R/W	MSB's lower nibble of the 6-byte destination addresss	0000	
1	Reserved	RO	-	--	
0	Bad FCS Generation	R/W	1 = Generate packets with bad FCS 0 = Generate packets with good FCS	0	

29E.15 - EPG Enable

When bit 29E.15 is set to a “1”, the EPG is selected as the driving source for the PHY transmit signals, and the MAC transmit pins are disabled. When bit 29E.15 is cleared, the MAC has full control of the PHY transmit signals.

29E.14 - EPG Run/Stop

Bit 29E.14 controls the beginning and end of packet transmission. When this bit is set to a “1”, the EPG begins the transmission of packets. When this bit is cleared, the EPG ends the transmission of packets, after the current packet is transmitted. Bit 29E.14 is valid only if bit 29E.15 is set to a “1”.

29E.13 - Transmission Duration

When bit 29E.13 is set to a “1”, the EPG will continuously transmit packets as long as bit 29E.14 is set to a “1”. If bit 29E.13 is cleared, the EPG will begin transmission of 30,000,000 packets when bit 29E.14 is set to a “1”, after which time, bit 29E.14 is automatically cleared. If bit 29E.13 changes during packet transmission, the new value will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a “1” again.

29E.12:11 - Packet Length

Bits 29E.12:11 select the length of the packets to be generated by the EPG. Note that when these bits are set to “11”, a 10,000-byte “jumbo” packet is sent, which may not be compatible with all Ethernet equipment. If bits 29E.12:11 change during packet transmission, the new values will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a “1” again.

29E.10 - Inter-packet Gap

Bit 29E.10 selects the inter-packet gap for packets generated by the EPG. If bit 29E.10 changes during packet transmission, the new value will not take effect until the EPG Run/Stop bit (29E.14) has been cleared and set to a “1” again.

25 Electrical Specifications

25.1 Absolute Maximum Ratings

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Symbol	Min	Max	Unit	Parameter Description & Conditions
P_D		3.4	W	Worst case power dissipation.
$T_{Storage}$	-65	150	°C	Storage temperature range.
T_J		+125	°C	Absolute maximum junction temperature.
$V_{DD(Analog)}$	-0.5	4.0	V	DC voltage on analog I/O supply pin.
$V_{DD(IO)}$	-0.5	4.0	V	DC voltage on any digital I/O supply pin.
$V_{DD(5V)}$	-0.5	5.5	V	DC voltage on any 5V-tolerant digital input pin.
$V_{DD(Dig-Core)}$	-0.5	1.5	V	DC voltage on any digital core supply pin.
$V_{DD(Analog-Core)}$	-0.5	1.5	V	DC voltage on any analog core supply pin.
$V_{Pin(DC)}$	-0.5	V_{DD} + 0.5	V	DC voltage on any non-supply pin.
$V_{ESD(HBM)}$	2		kV	ESD voltage on any pin, per event, according to the Human Body Model.
CESD	2		kV	Cable-sourced ESD tolerance, per event, at 200 meters.
$I_{LATCHUP}$	-200	+200	mA	T = +85°C, valid for all I/O signal pins.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

25.2 Recommended Operating Conditions

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
VDD33	3.0	3.3	3.6	V	DC voltage on VDD33 pins
$VDDIO_{MAC}$	3.0 2.3 1.4	3.3 2.5 1.5	3.6 2.7 1.6	V	DC voltage on $VDDIO_{MAC}$ pins[1]
$V_{REF\ (HSTL)}$	.68	.75	.90	V	HSTL I/O reference voltage
$VDDIO_{micro}$	3.0 2.3 1.4	3.3 2.5 1.5	3.6 2.7 1.6	V	DC voltage on $VDDIO_{micro}$ pins[1]
$VDDIO_{ctl}$	3.0 2.3	3.3 2.5	3.6 2.7	V	DC voltage on $VDDIO_{ctl}$ pins[1]
VDD12	1.14	1.2	1.26	V	DC voltage on VDD12 pins
VDDDIG	1.14	1.2	1.26	V	Digital core logic DC power supply voltage.
F_{REFCLK}		25 125		MHz	Local reference clock (REFCLK) nominal frequency. Refer to F_{TOL} for min and max values.
$F_{TOL\ (REFCLK)}$	-100		+100	ppm	Reference clock frequency offset tolerance over specified temperature range (25MHz or 125MHz)[2]
$F_{TOL\ (LINK)}$	-1500		+1500	ppm	Link partner frequency offset tolerance (for any link speed)[2]
R_{EXT}		2.00		kΩ	External reference circuit bias resistor (1% tolerance).
C_{REF_FILT}		1.0		µF	External reference generator filter capacitor (10% tolerance).
$T_{(OPER)}$	0		100	°C	Lower limit of specification is ambient temperature, and upper limit is case temperature.

[1] On-chip I/O calibration only valid within these recommended operating conditions.

[2] Refer to the Applications Note *Using Jumbo Packets with SimpliPHYs* for further information about clocking and frequency offset tolerance specifications when jumbo packet support is required.

25.3 Thermal Application Data

Printed Circuit Board Conditions (JEDEC JESD51-9)		
PCB Layers	6	4
PCB Dimensions (mm x mm)	101.6 x 114.3	101.6 x 114.3
PCB Thickness (mm)	1.6	1.6
Environment Conditions		
Maximum operation junction temperature (ºC)	125	125
Ambient free-air operating temperature (ºC)	70	70
Worst Case Power Dissipation (W)	3.4	3.4

25.4 Package Thermal Specifications - 260 HS-PBGA

Table 39. Thermal Air Flow Specifications - 260 ball HSBGA 19mm package

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
θ_{JA} (0 m/s air-flow)		17.5 20.2		°C/W	Junction-to-ambient thermal resistance 6-layer 4-layer
θ_{JA} (1 m/s air-flow)		14.8 17.5		°C/W	Junction-to-ambient thermal resistance 6-layer 4-layer
θ_{JA} (2 m/s air-flow)		13.8 16.2		°C/W	Junction-to-ambient thermal resistance 6-layer 4-layer

Table 40. Thermal Specifications - 260 ball HSBGA 19mm package

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_A			70	°C	Ambient free-air operating temperature
T_J			125	°C	Maximum operating junction temperature
θ_{JC}		5.1 5.2		°C/W	Junction-to-case thermal resistance 6-layer 4-layer
Ψ_{JT}		4.47 4.61		°C/W	Junction-to-top center of case thermal resistance 6-layer 4-layer
θ_{JB}		10.4 12.2		°C/W	Junction-to-board thermal resistance 6-layer 4-layer

25.5 Current and Power Consumption Estimates

Typical power supply current and power consumption information is provided below for PCB design targets. All typical data below is based on engineering measurements at nominal voltages with 1000BASE-T RGMII, 64-byte random data pattern under 100% utilization in full-duplex mode. A maximum margin of ±20% should be included to account for variation in the specified power supply voltage ranges, as well as for variation due to the normal silicon process spread and temperature conditions.

Table 41. Current and Power Consumption Estimates - HSTL @ 1.5V, RGMII mode, no LEDs, no CLK125

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33}		397		mA	Analog 3.3V power supply current into VDD33 pins
$I_{VDDIOMAC}$		50		mA	Digital I/O supply current into $VDDIO_{MAC}$ @ 1.5V
$I_{VDDIOmicro}$		0.3		mA	Digital I/O supply current into $VDDIO_{micro}$ @ 3.3V
$I_{VDDIOctl}$		2.5		mA	Digital I/O supply current into $VDDIO_{ctl}$ @ 3.3V
I_{VDD12}		136		mA	Analog 1.2V power supply current into VDD12 pins
I_{VDDDIG}		821		mA	Digital 1.2V core power supply current into VDDDIG pins
P_D		636		mW	Power dissipation per port (no LEDs)

Table 42. Current and Power Consumption Estimates - 2.5V, RGMII mode, no LEDs, no CLK125

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33}		397		mA	Analog 3.3V power supply current into VDD33 pins
$I_{VDDIOMAC}$		98.6		mA	Digital I/O supply current into $VDDIO_{MAC}$ @ 2.5V
$I_{VDDIOmicro}$		0.3		mA	Digital I/O supply current into $VDDIO_{micro}$ @ 3.3V
$I_{VDDIOctl}$		2.5		mA	Digital I/O supply current into $VDDIO_{ctl}$ @ 3.3V
I_{VDD12}		136		mA	Analog 1.2V power supply current into VDD12 pins
I_{VDDDIG}		821		mA	Digital 1.2V core power supply current into VDDDIG pins
P_D		679		mW	Power dissipation per port (no LEDs)

Table 43. Current and Power Consumption Estimates - 3.3V, RGMII mode, no LEDs, no CLK125

Symbol	Min	Typ	Max	Unit	Description
I_{VDD33}		397		mA	Analog 3.3V power supply current into VDD33 pins
$I_{VDDIOMAC}$		149		mA	Digital I/O supply current into $VDDIO_{MAC}$ @ 3.3V
$I_{VDDIOmicro}$		0.3		mA	Digital I/O supply current into $VDDIO_{micro}$ @ 3.3V
$I_{VDDIOctl}$		2.5		mA	Digital I/O supply current into $VDDIO_{ctl}$ @ 3.3V
I_{VDD12}		136		mA	Analog 1.2V power supply current into VDD12 pins
I_{VDDDIG}		821		mA	Digital 1.2V core power supply current into VDDDIG pins
P_D		740		mW	Power dissipation per port (no LEDs)

25.6 DC Specifications

25.6.1 Digital Pins Referenced to VDDIO = 3.3V

The specifications listed in Table 44 and Table 45 are valid only when $T_{Ambient}$ = 25°C, VDDIO = 3.3V, VDDDIG = 1.2V, VDD33 = 3.3V, VSSIO = 0V, and VSSS = 0V.

Table 44. Digital Pins Specifications (VDDIO = 3.3V)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
V_{OH}	2.1		VDDIO + 0.3	V	Output high voltage. VDDIO = MIN, I_{OH} = -1.5mA
V_{OL}	GND		0.5	V	Output low voltage. VDDIO = MIN, I_{OL} = 1.5mA
V_{IH}	2.0			V	Input high voltage.
V_{IL}			0.9	V	Input low voltage.
I_{ILeak}	-10		10	µA	Input leakage current.
I_{OLeak}	-10		10	µA	Output leakage current.
I_{OL}			12	mA	Output low current drive strength
I_{OH}	-12			mA	Output high current drive strength
Z_O		50		Ω	Output driver impedance

25.6.2 Digital Pins Referenced to VDDIO = 2.5V

Table 45. Digital Pins Specifications (VDDIO = 2.5V)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
V_{OH}	2.0		VDDIO + 0.3	V	Output high voltage. VDDIO = MIN, I_{OH} = -1.0mA
V_{OL}	GND - 0.3		0.4	V	Output low voltage. VDDIO = MIN, I_{OL} = 1.0mA
V_{IH}	1.7			V	Input high voltage. VDDIO = MIN
V_{IL}			0.7	V	Input low voltage. VDDIO = MIN
I_{ILeak}	-10		10	µA	Input leakage current.
I_{OLeak}	-10		10	µA	Output leakage current.
I_{OL}			12	mA	Output low current drive strength
I_{OH}	-12			mA	Output high current drive strength
Z_O		50		Ω	Output driver impedance

25.6.3 Digital Pins (VDDIO = 1.5V HSTL)

The following specifications are valid only when $T_{Ambient}$ = 25°C, VDDIO = 1.5V, VDDDIG = 1.2V, VDD33 = 3.3V, VSSIO = 0V, and VSSS = 0V.

Table 46. Digital Pins Specifications (VDDIO = 1.5V)

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
V_{OH}	VDDIO - 0.4			V	Output high voltage VDDIO = MIN, I_{OH} = -1.0mA
V_{OL}			0.4	V	Output low voltage VDDIO = MIN, I_{OL} = 1.0mA
V_{IH}	VREF + 0.12		VDDIO + 0.3	V	Input high voltage VDDIO = MIN
V_{IL}	- 0.3		VREF - 0.12	V	Input low voltage VDDIO = MIN
I_{ILeak}		10		µA	Input leakage current
I_{OLeak}		10		µA	Output leakage current
I_{OL}			12	mA	Output low current drive strength
I_{OH}	-12			mA	Output high current drive strength
Z_O		50		Ω	Output driver impedance

25.6.4 LED Output Pins (LED[4:0]_n)

The following specifications are valid over a voltage range of 2.3V to 1.3V applied to the LED pins.

Table 47. LED Output Pins Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
I_{ILeak}		10		µA	Input leakage current
I_{OLeak}		10		µA	Output leakage current
I_{OL}			18	mA	Output low current drive strength
I_{OH}	-18			mA	Output high current drive strength
Z_O		50		Ω	Output driver impedance

25.7 Clocking Specifications

25.7.1 Reference Clock Option

The following component specifications should be used to select a clock reference for use with the VSC8244[1].

Table 48. Reference Clock Option Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$F_{TOL-25MHZ}$	-100 ppm	25	+100 ppm	MHz	Total frequency offset tolerance (25MHz clock option), including, initial offset, stability over temperature.
$T_{R1,}$ T_{F1}			4	ns	Rise and fall time (20% to 80%), 25MHz clock option.
$T_{R2,}$ T_{F2}			0.8	ns	Rise and fall time (20% to 80%), 125MHz clock option.
DUTY	45		55	%	Duty cycle (25MHz and 125MHz clock options).

[1]Refer to the Applications Note *Using Jumbo Packets with SimpliPHYs* for further information about clocking and frequency offset tolerance specifications when jumbo packet support is required.

25.7.2 Crystal Option

The following component specifications should be used to select a crystal for use with the VSC8244[1]. Refer to the Application Note *Using Jumbo Packets with SimpliPHYs* for further information about clocking and frequency offset tolerance specifications when jumbo packet support is required.

Table 49. Crystal Option Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
F_{REF}		25		MHz	Fundamental mode, AT-cut type, parallel resonant crystal reference frequency.
$F_{TOL(TOTAL)}$	-50		+50	ppm	Fundamental mode, AT-cut type, parallel resonant crystal total frequency offset, including, initial offset, stability over temperature, aging and capacitive loading
C_L	18		20	pF	Crystal parallel load capacitance.
C_{L-EXT}		33		pF	Crystal external load capacitors (C1 and C2) to GND[1]
ESR		10	30	Ω	Equivalent Series Resistance of crystal.
P_D			0.5	mW	Crystal oscillator drive level.

[1] These values can depend on board parasitics.

25.8 System Timing Specifications

25.8.1 RGMII Mode Timing

For RGMII mode, the following specifications are valid when the I/O power supply ($VDDIO_{MAC}$) is 1.5V, 2.5V, or 3.3V, ±5%, per the RGMII v2.0 specification, and the MAC I/F selection bits have been set to RGMII mode. See MII Register bit 23.11:8 and the RGMII specification for more information.

Table 50. RGMII Mode AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{skew}T$	-500	0	500	ps	Data to clock output skew (at PHY) – uncompensated mode.
$T_{skew}R$	1	1.8	2.6	ns	Data to clock output skew (at receiver) – uncompensated mode.[1]
$T_{setup}T$	1.2	2.0	0	ns	Data to clock output Setup (at PHY integrated delay)[2]
$T_{hold}T$	1.2	2.0	0	ns	Data to clock output Setup (at transmitter integrated delay)[2]
$T_{setup}R$	1.0	2.0	0	ns	Data to clock output Setup (at receiver integrated delay)[2]
$T_{hold}R$	1.0	2.0	0	ns	Data to clock output Setup (at PHY integrated delay)[2]
$T_{CYC1000}$ T_{CYC100} T_{CYC10}	7.2 36 360	8 40 400	8.8 44 440	ns	Clock cycle duration.
$Duty_{1000}$	45	50	55	%	Duty cycle for 1000BASE-T.[3]
$Duty_{10/100}$	40	50	60	%	Duty cycle for 10BASE-T and 100BASE-TX.[3]
T_R, T_F			.75	ns	Rise, fall time (20% to 80%).

Table 50. RGMII Mode AC Timing Specifications *(continued)*

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$V_{thresh1.5}$ $V_{thresh2.5}$ $V_{thresh3.3}$		0.75 1.25 1.65		V V V	TX_CLK_n Switching Threshold based on VDD_{MAC}

[1] This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal. This is normal operating mode (RGMII timing is not compensated). To enable RGMII timing compensation, see MII Register 23.11:8.

[2] RGMII-ID mode (RGMII with Internal Delay Compensation On) - a 2ns delay is added to the TX_CLK_n and RX_CLK_n signals inside the PHY.

[3] Duty cycle may be stretched or shrunk during speed changes or while transitioning to a received packet's clock domain, as long as the minimum duty cycle is not violated, and stretching occurs for no more than three T_{CYC} of the lowest speed transitioned between.

Figure 27 diagrams RGMII timing and multiplexing in uncompensated mode.

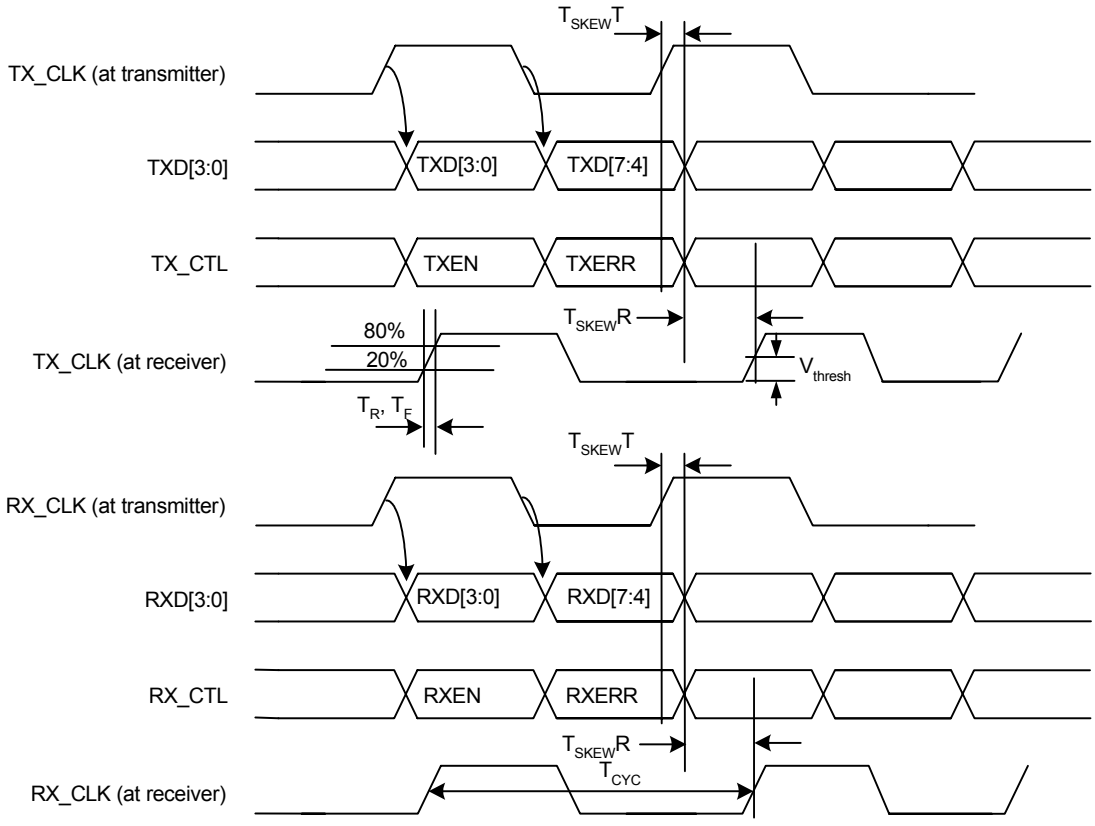


Figure 27. RGMII Uncompensated AC Timing and Multiplexing

The RGMII specification (v2.0) defines the following relationship between the clock and data signals at the MAC/PHY interface:

To meet this timing specification, a 1.5ns delay to the TX_CLK_n and RX_CLK_n signals is typically added on the PC board using a long "trombone shaped" trace.

The VSC8244 also includes an optional mode of operation where the PCB delay is handled internally (on-chip). This operating mode can be enabled by setting MII Register 23.11:8 high. In this operation mode, the VSC8244 expects the following relationship between TX_CLK_n and TD on the transmit side and RX_CLK_n and RD on the receive side:

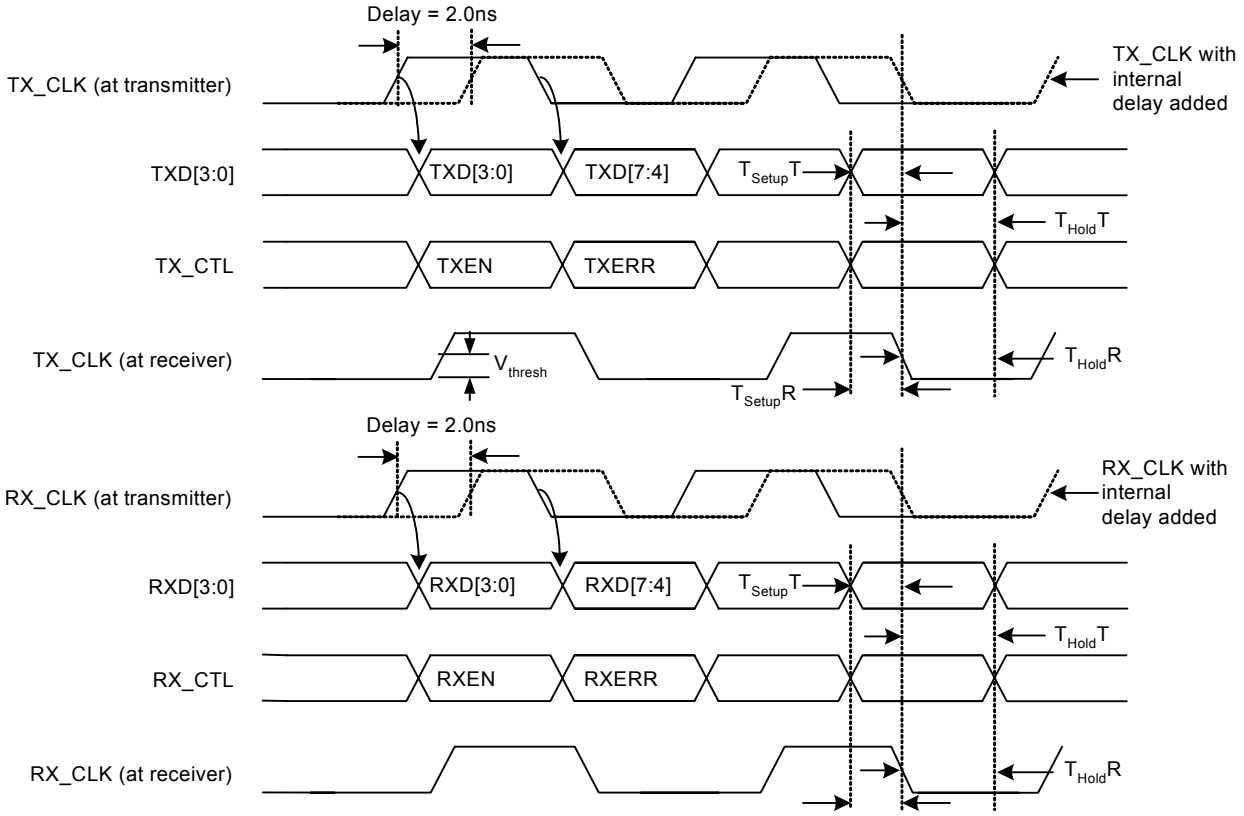


Figure 28. RGMII Compensated AC Timing and Multiplexing

Since no “trombone shaped” traces are required with this approach, the advantages of this compensated timing of RGMII v2.0 include:

- Simplified board design
- More compact routes; less board area
- Lower EMI emissions
- Greater distance possible between the MAC and PHY
- Improved signal integrity for a given distance between the MAC and PHY.

25.8.2 RTBI Mode Timing

For RTBI mode, the following specifications are valid when the I/O power supply ($VDDIO_{MAC}$) is 1.5V, 2.5V, or 3.3V, ±5%, per the RGMII (v2.0) specification, and the MAC I/Fselection bits have been set to RTBI mode. See MII Register bit 23.11:8 and the RTBI specification for more information.

Table 51. RTBI Mode AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{skew}T$	-500	0	500	ps	Data to clock output skew (at PHY) – uncompensated mode.
$T_{skew}R$	1	1.8	2.6	ns	Data to clock output skew (at receiver) – uncompensated mode.[1]
$T_{setup}T$	1.2	2.0	0	ns	Data to clock output Setup (at PHY integrated delay)[2]
$T_{hold}T$	1.2	2.0	0	ns	Data to clock output Setup (at transmitter integrated delay)[2]
$T_{setup}R$	1.0	2.0	0	ns	Data to clock output Setup (at receiver integrated delay)[2]
$T_{hold}R$	1.0	2.0	0	ns	Data to clock output Setup (at PHY integrated delay)[2]
$T_{CYC1000}$ T_{CYC100} T_{CYC10}	7.2 36 360	8 40 400	8.8 44 440	ns	Clock cycle duration.
$Duty_{1000}$	45	50	55	%	Duty cycle for 1000BASE-T.[3]
$Duty_{10/100}$	40	50	60	%	Duty cycle for 10BASE-T and 100BASE-TX.[3]
$T_{R,}$ T_F			.75	ns	Rise, fall time (20% to 80%).
$V_{thresh1.5}$ $V_{thresh2.5}$ $V_{thresh3.3}$		0.75 1.25 1.65		V V V	TX_CLK_n Voltage Threshold based on $VDDIO_{MAC}$

[1] This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal. This is normal operating mode (RTBI timing is not compensated). To enable RGMII timing compensation, see MII Register 23.11:8.

[2] RTBI compensated mode (RGMII with Internal Delay Compensation On) - a 2ns delay is added to the TX_CLK_n and RX_CLK_n signals inside the PHY.

[3] Duty cycle may be stretched or shrunk during speed changes or while transitioning to a received packet's clock domain, as long as the minimum duty cycle is not violated, and stretching occurs for no more than three T_{CYC} of the lowest speed transitioned between.

Figure 29 diagrams RTBI timing and multiplexing in uncompensated mode.

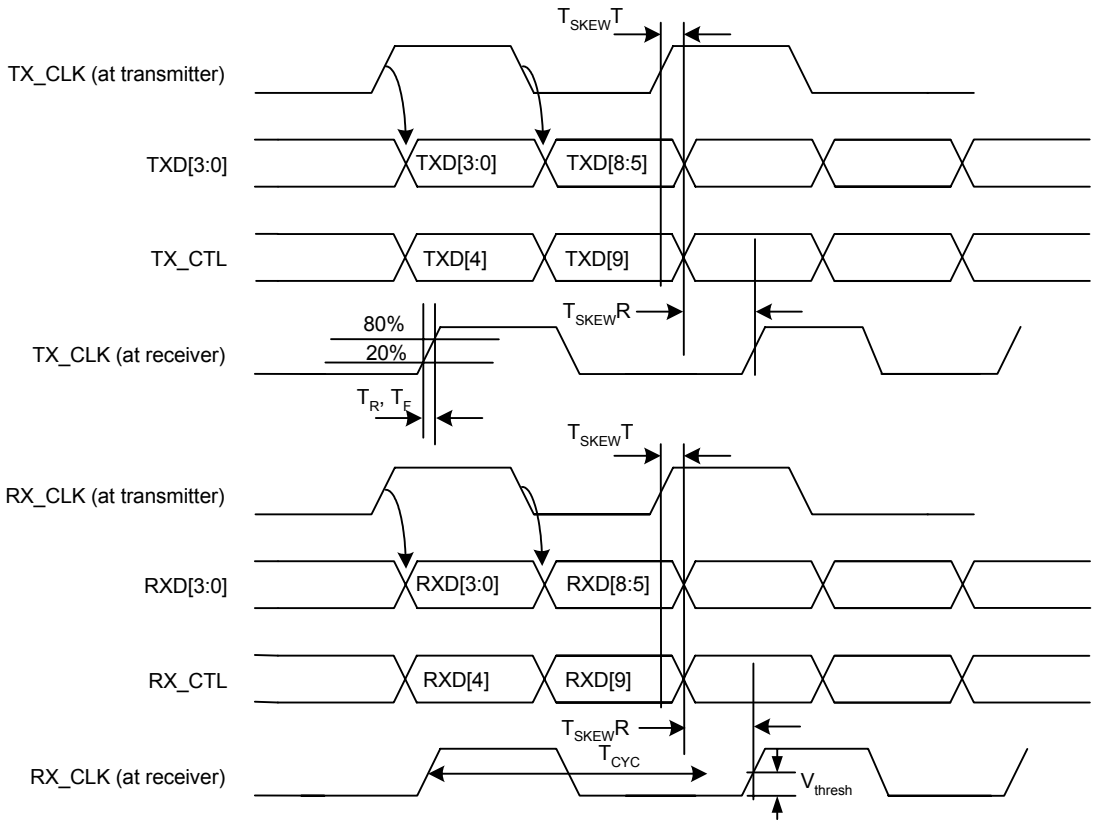


Figure 29. RTBI Uncompensated AC Timing and Multiplexing

The RGMII specification (v2.0) defines the following relationship between the clock and data signals at the MAC/PHY interface:

To meet this timing specification, a 1.5ns delay to the TX_CLK_n and RX_CLK_n signals is typically added on the PC board using a long “trombone shaped” trace.

The VSC8244 also includes a mode of operation where the addition of this delay is handled internally. This operating mode can be enabled by setting MII Register 23.11:8 high. In this operation mode, the VSC8244 expects the following relationship between TX_CLK_n and TD on the transmit side and RX_CLK_n and RD on the receive side:

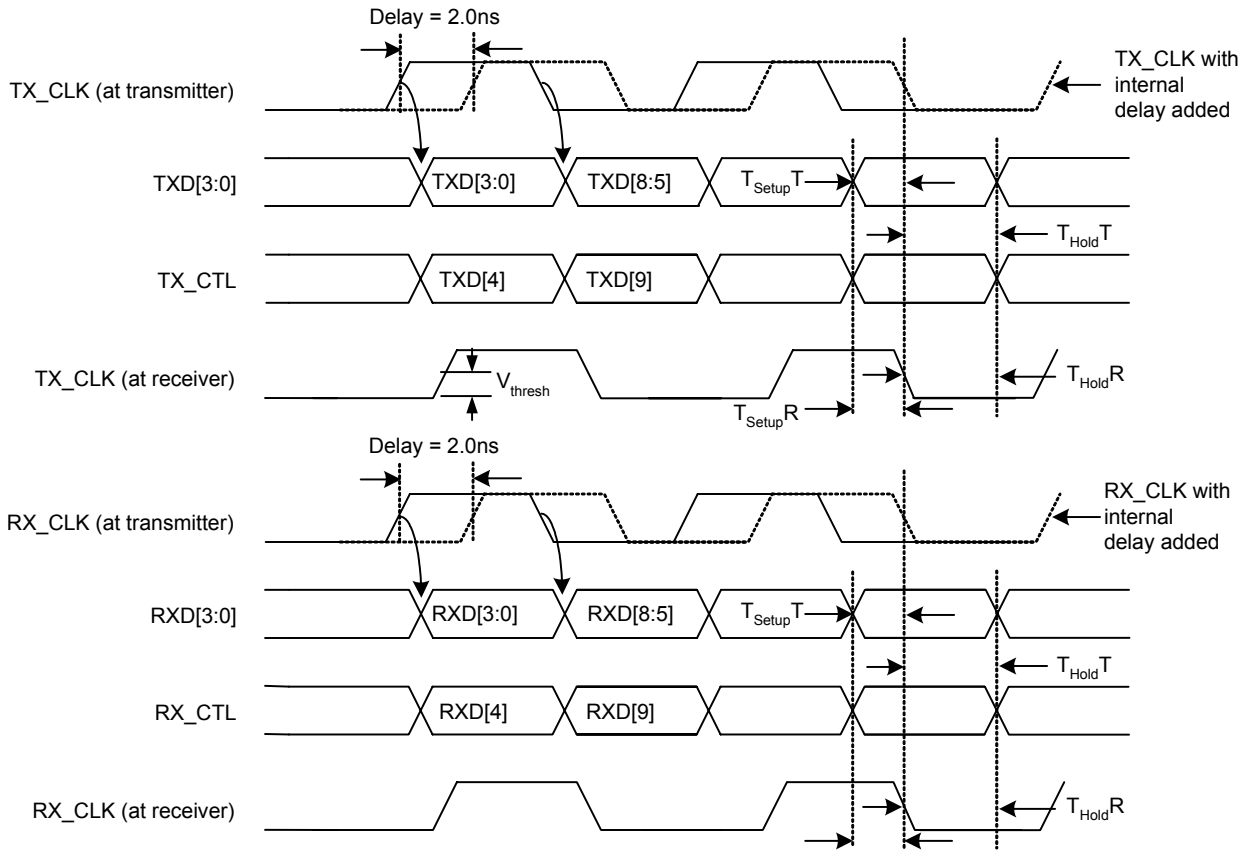


Figure 30. RTBI Compensated AC Timing and Multiplexing

Since no “trombone shaped” trace is required with this approach, the advantages of this compensated timing over RGMII v2.0 include:

- Simplified board design
- More compact routes; less board area
- Lower EMI emissions
- Greater distance possible between the MAC and PHY
- Improved signal integrity for a given distance between the MAC and PHY.

25.8.3 JTAG Timing

The following specifications are valid only when the I/O power supply ($VDDIO_{ctl}$) is at either 3.3V, ±5%, or 2.5V, ±5%.

Table 52. JTAG Interface AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{TCK-Period}$	100			ns	TCK period.
$T_{TCK-High}$	45			ns	TCK minimum pulse width high.
$T_{TCK-Low}$	45			ns	TCK minimum pulse width low.
$T_{TDI/TMS-Setup}$	10			ns	(TMS or TDI) to TCK setup time.
$T_{TDI/TMS-Hold}$	10			ns	(TMS or TDI) to TCK hold time.
$T_{TDO-Delay}$			15	ns	TDO delay from TCK.

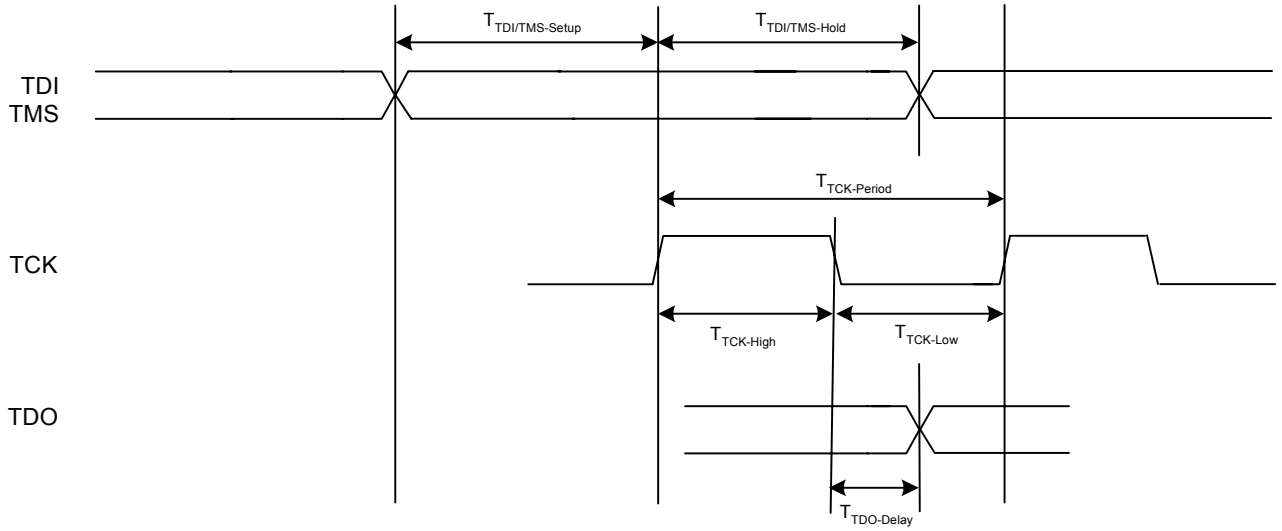


Figure 31. JTAG Interface AC Timing

25.8.4 SMI Timing

The following specifications are valid only when the I/O power supply ($VDDIO_{micro}$) is at either 3.3V, ±5%, or 2.5V, ±5%.

Table 53. SMI AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
F_{MDC}	0	2.5	12.5	MHz	MDC clock frequency.
$T_{MDC-High}$	20	50		ns	MDC clock pulse width high.
$T_{MDC-Low}$	20	50		ns	MDC clock pulse width low.
$T_{MDIO-Setup}$	10			ns	MDIO to MDC setup time when sourced by Station Manager.
$T_{MDIO-Hold}$	10			ns	MDIO to MDC hold time when sourced by Station Manager.
T_R,T_F	100 T_{MDC} x 10%[1]			ns	MDC rise and fall time. For MDC = 0 - 1MHz For MDC = 1MHz - F_{MDC}(MAX)
$T_{MDIO-Delay}$		10	300	ns	MDC to MDIO delay time from VSC8244. Delay will depend on value of external pull-up resistor on MDIO pin.

[1] For F_{MDC} above 1MHz, the minimum rise and fall times are in relation to the frequency of the MDC clock period. Example: if F_{MDC} = 2MHz, then the minimum T_R/T_F is 50ns.

Note: At 16MHz, a 400Ω pull-up resistor on the MDIO pin is recommended; otherwise, a 2kΩ pull-up resistor is recommended at 2MHz.

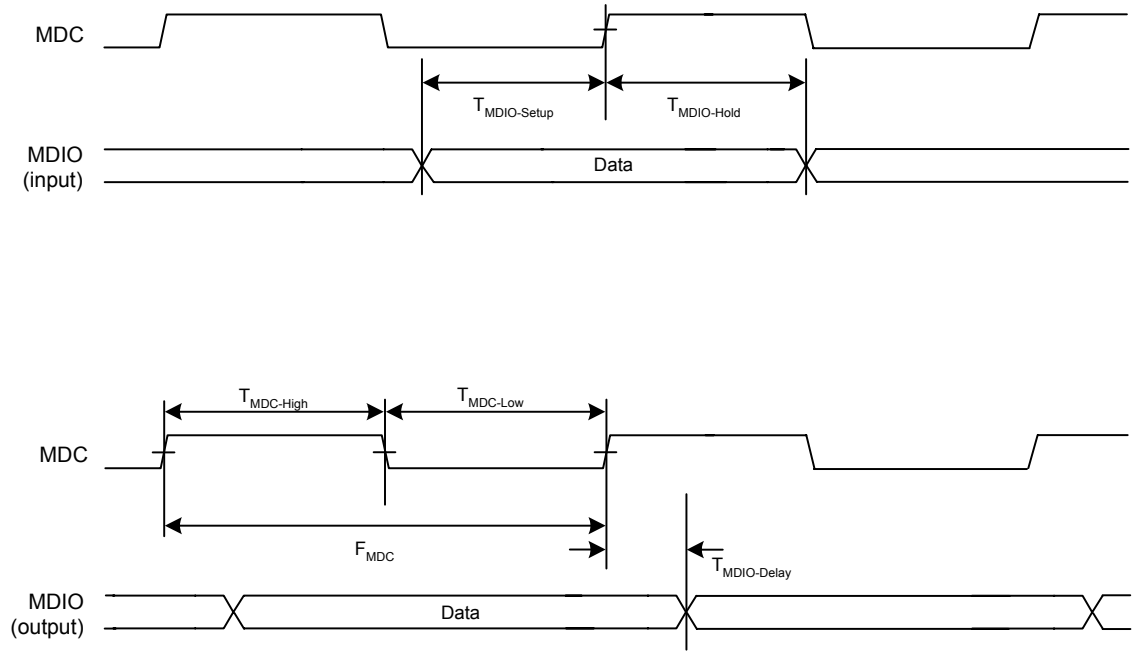


Figure 32. SMI AC Timing

25.8.5 $\overline{\text{MDINT}}$ Timing

The following specifications are valid only when the I/O power supply ($VDDIO_{micro}$) is at either 3.3V, ±5%, or 2.5V, ±5%.

Table 54. $\overline{\text{MDINT}}$ AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
t_F			110	ns	$\overline{\text{MDINT}}$ fall time, assuming a 2.2kΩ external pull-up resistor and a 50pF total capacitive load.

25.8.6 Serial LED_CLK and LED_DATA Timing

The following specifications are valid only when the I/O power supply (VDD33) is at either 3.3V, ±5%, or 2.5V, ±5%.

Table 55. LED_CLK and LED_DATA Output AC Timing Specification

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_{LED_CLK}	1			µs	LED_CLK output period.
$T_{LED\_CLK\text{-}Pause}$	25			ms	LED_CLK pause between LED bit sequence repeat (un-preambled mode).
$T_{LED\_DATA\text{-}Delay}$			15	ns	LED_DATA propagation delay from rising edge of LED_CLK.

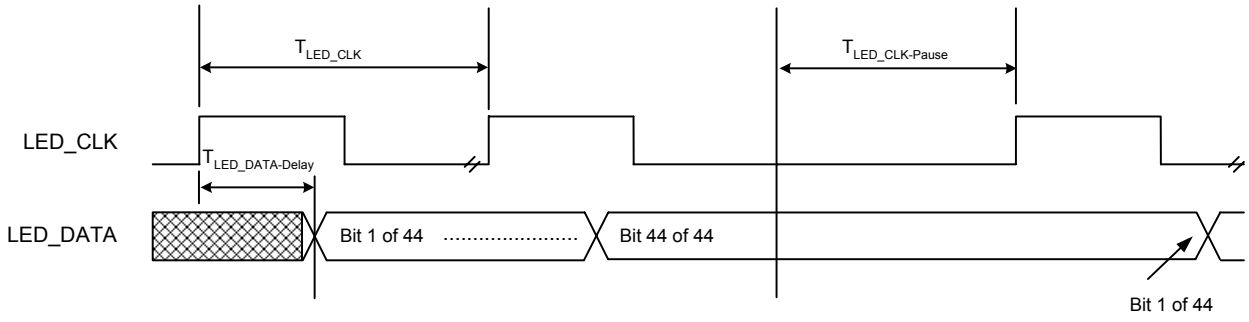


Figure 33. LED_CLK and LED_DATA Output AC Timing

25.8.7 REFCLK Timing

The following specifications are valid only when the I/O power supply (VDD33) is at either 3.3V, ±5%, or 2.5V, ±5%. Refer to the Application Note *Using Jumbo Packets with SimpliPHYs* for further information about clocking and frequency offset tolerance specifications when jumbo packet support is required.

Table 56. REFCLK AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{REFCLK25}$		40		ns	Reference clock period, PLLMODE = 0 (25MHz reference).
$T_{REFCLK125}$		8		ns	Reference clock period, PLLMODE = 1 (125MHz reference).
$F_{STABILITY}$			50	ppm	Reference clock frequency stability (0°C to 70°C).
T_{DUTY}	40	50	60	%	REFCLK duty cycle in both 25MHz and 125MHz modes.
$J_{REFCLK25}$, $J_{REFCLK125}$			300	ps	Total jitter of 25MHz or 125MHz reference clock (peak-to-peak).
$t_{R/F\ (REFCLK25)}$			4	ns	Reference clock rise time, 25MHz mode (20% to 80%).
$t_{R/F\ (REFCLK125)}$			1	ns	Reference clock rise time, 125MHz mode (20% to 80%).

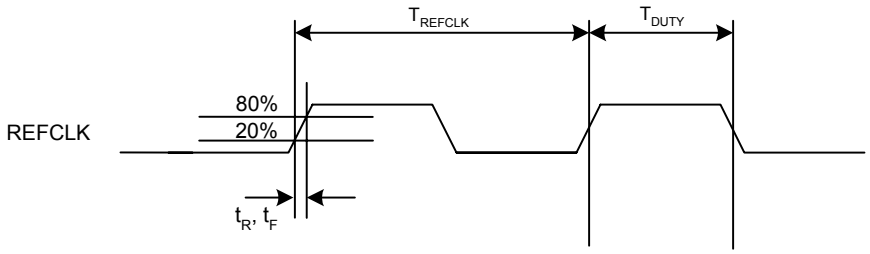


Figure 34. REFCLK AC Timing

25.8.8 CLK125$_{MAC}$ and CLK125$_{micro}$ Timing

The following specifications are valid only when the I/O power supply (VDDIO$_{MAC}$ for CLK125$_{MAC}$) is at either 3.3V ±5%, 2.5V ±5%, or 1.5V ±5%.
The following specifications are valid only when the I/O power supply (VDDIO$_{micro}$ for CLK125$_{micro}$) is at either 3.3V ±5%, or 2.5V ±5%.

Table 57. CLK125 AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{CLK125MAC}$		8		ns	Reference clock period.
$T_{CLK125micro}$		250 8		ns	Reference clock period. Either 4MHz, or 125MHz
$F_{STABILITY}$			50	ppm	Reference clock frequency stability (0°C to 70°C).
T_{DUTY}	40	50	60	%	Reference clock duty cycle.
J_{CLK125}			300	ps	Total jitter of reference clock (peak-to-peak).
$t_{R/F\ (CLK125)}$			1	ns	Reference clock rise time (20% to 80%).

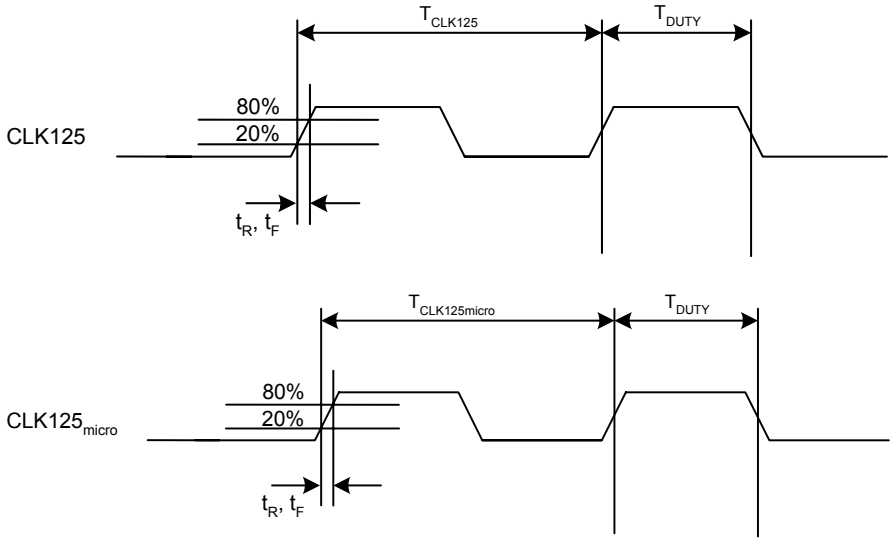


Figure 35. CLK125 AC Timing

25.8.9 Reset Timing

The following specifications are valid only when the I/O power supply (VDDIOmicro) is at either 3.3 V, ±5%, or 2.5 V, ±5%.

Table 58. $\overline{\text{RESET}}$ AC Timing Specification

Symbol	Min	Typ	Max	Unit	Description	Conditions
T_{RESET}	100			ns	Reset assertion time	
T_{READY}		13	20	ms	Reset to SMI active time	

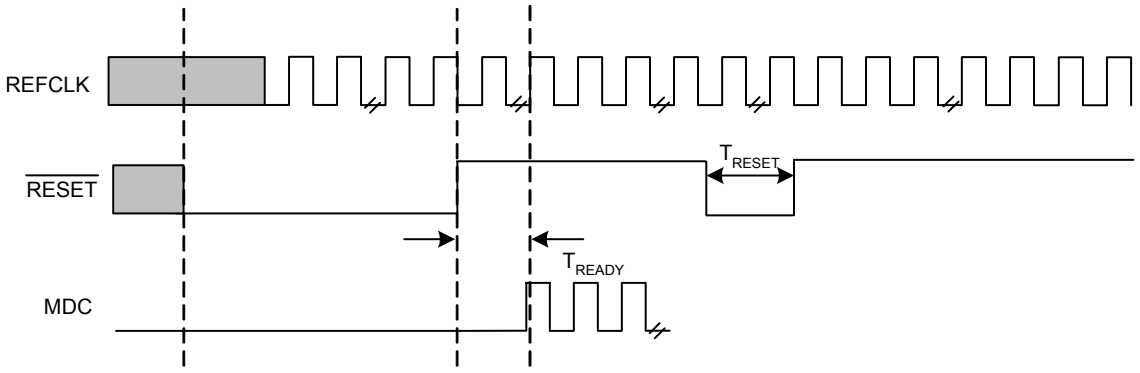


Figure 36. $\overline{\text{RESET}}$ AC Timing

26 Packaging Specifications

26.1 19mm HS-PBGA Mechanical Specification

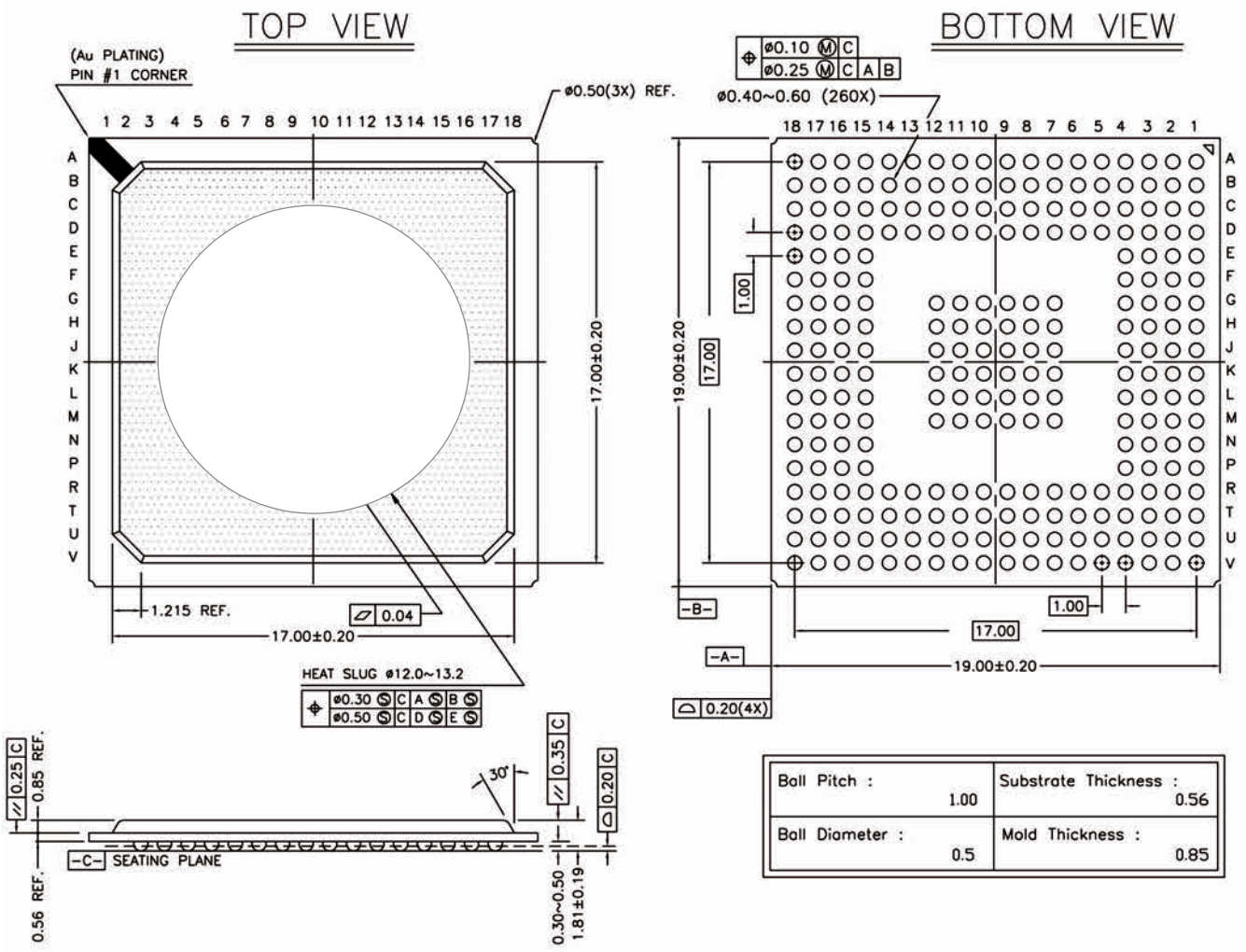


Figure 37. 19mm HS-PBGA Mechanical Specification

26.2 Package Moisture Sensitivity

Moisture sensitivity level ratings for Vitesse products comply with the joint IPC and JEDEC standard IPC/JEDEC J-STD-020.

VSC8244HG is rated moisture sensitivity level 3 or better.

VSC8244XHG is rated moisture sensitivity level 4.

For more information, see the IPC and JEDEC standard.

27 Ordering Information

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

27.1 Devices

Part Number	Package Type	Description
VSC8244HG	260 HS-PBGA 1mm ball pitch 19x19mm body	Quad 10/100/1000BASE-T PHY with RGMII and RTBI interfaces
VSC8244XHG	260 HS-PBGA 1mm ball pitch 19x19mm body	Lead(Pb)-free, quad 10/100/1000BASE-T PHY with RGMII and RTBI interfaces

27.2 Related Devices

Part Number	Package Type	Description
VSC8224HG	260 HS-PBGA 1mm ball pitch 19x19mm body	Quad 10/100/1000BASE-T and 1000BASE-X PHY with RGMII/RTBI interfaces
VSC8224XHG	260 HS-PBGA 1mm ball pitch 19x19mm body	Lead(Pb)-free, quad 10/100/1000BASE-T and 1000BASE-X PHY with RGMII/RTBI interfaces
VSC8234HG	260 HS-PBGA 1mm ball pitch 19x19mm body	Quad 10/100/1000BASE-T PHY with SGMII/1000BASE-X SerDes MAC interfaces
VSC8234XHG	260 HS-PBGA 1mm ball pitch 19x19mm body	Lead(Pb)-free, quad 10/100/1000BASE-T PHY with SGMII/1000BASE-X SerDes MAC interfaces

28 Design Guidelines

The complete set of support documentation for the VSC8244, including a text file that can be used as the startup script, is available on the Vitesse web site, https://www.vitesse.com. Access to some documents may require the filing of a non-disclosure agreement.

28.1 Required SMI Register Write Sequence

At initialization, a number of internal registers must be changed from their default values.

A series of register writes must be executed after each device power-up or reset. A microcontroller or a startup configuration EEPROM (connected to the device as described in Section 22.4.2, “Programming Multiple VSC8244 using the same EEPROM,” on page 56, must be included in the system design).

The register rewrites are listed in Section 22.4: "EEPROM Interface".

In executing the writes, use the format: smiwrite[PHY, register, data]. All register and data values listed in the table are in hexadecimal notation.

Table 59. Startup Write Sequence Changes

	PHY	Register	Data		PHY	Register	Data
smiwrite	0	1F	2A30	smiwrite	2	1F	2A30
smiwrite	0	08	0212	smiwrite	2	08	0212
smiwrite	0	1F	52B5	smiwrite	2	1F	52B5
smiwrite	0	10	AFA4	smiwrite	2	10	AFA4
smiwrite	0	12	000F	smiwrite	2	12	000F
smiwrite	0	11	492A	smiwrite	2	11	492A
smiwrite	0	10	8FA4	smiwrite	2	10	8FA4
smiwrite	0	1F	2A30	smiwrite	2	1F	2A30
smiwrite	0	08	0012	smiwrite	2	08	0012
smiwrite	1	1F	2A30	smiwrite	3	1F	2A30
smiwrite	1	08	0212	smiwrite	3	08	0212
smiwrite	1	1F	52B5	smiwrite	3	1F	52B5
smiwrite	1	10	AFA4	smiwrite	3	10	AFA4
smiwrite	1	12	000F	smiwrite	3	12	000F
smiwrite	1	11	492A	smiwrite	3	11	492A
smiwrite	1	10	8FA4	smiwrite	3	10	8FA4
smiwrite	1	1F	2A30	smiwrite	3	1F	2A30
smiwrite	1	08	0012	smiwrite	3	08	0012

28.2 Interoperability with Intel 82547E1 L322SQ96

The Intel 82547E1 PHY, by design, links in slave mode with over 99% probability and then changes its operating mode to a non-IEEE-compliant manner shortly after responding to a master link partner’s initial transmission. The timing of this event is such that, over cabling shorter than approximately 2 meters in length, the affected link partner drops the link and attempts to link again. This cycle can repeat indefinitely.

A series of register writes must be executed after each device power-up or reset. A microcontroller or a startup configuration EEPROM (connected to the device as described in Section 22.4.2, “Programming Multiple VSC8244 using the same EEPROM,” on page 56, must be included in the system design).

The register rewrites are listed in Section 22.4: "EEPROM Interface".

In executing the writes, use the format: smiwrite[PHY, register, data]. All register and data values listed in the table are in hexadecimal notation.

Table 60. Startup Write Sequence Changes for Intel 82547E1 Interoperability

	PHY	Register	Data		PHY	Register	Data
smiwrite	0	1F	2A30	smiwrite	2	1F	2A30
smiwrite	0	08	0212	smiwrite	2	08	0212
smiwrite	0	1F	52B5	smiwrite	2	1F	52B5
smiwrite	0	12	0004	smiwrite	2	12	0004
smiwrite	0	11	0671	smiwrite	2	11	0671
smiwrite	0	10	8FAE	smiwrite	2	10	8FAE
smiwrite	0	1F	2A30	smiwrite	2	1F	2A30
smiwrite	0	08	0012	smiwrite	2	08	0012
smiwrite	0	1F	0000	smiwrite	2	1F	0000
smiwrite	0	12	0049	smiwrite	2	12	0049
smiwrite	1	1F	2A30	smiwrite	3	1F	2A30
smiwrite	1	08	0212	smiwrite	3	08	0212
smiwrite	1	1F	52B5	smiwrite	3	1F	52B5
smiwrite	1	12	0004	smiwrite	3	12	0004
smiwrite	1	11	0671	smiwrite	3	11	0671
smiwrite	1	10	8FAE	smiwrite	3	10	8FAE
smiwrite	1	1F	2A30	smiwrite	3	1F	2A30
smiwrite	1	08	0012	smiwrite	3	08	0012
smiwrite	1	1F	0000	smiwrite	3	1F	0000
smiwrite	1	12	0049	smiwrite	3	12	0049

29 Product Support

All support documents for the VSC8244 can be accessed on the SiteStation website at http://design.vitesse.com. Access to some documents may require the filing of non-disclosure agreement with Vitesse.

29.1 Available Documents and Application Notes

- Startup Script File (At initialization, a number of internal registers must be changed from their default values. See VSC8244 Rev C startup script text file).
- IBIS Model
- OrCAD Symbol
- BSDL File
- Package Pinout Excel Spreadsheet File
- Design & Layout Guidelines - Applications Note
- SimpliPHY'd Magnetics for EMI Control - Applications Note
- Using Jumbo Packets with SimpliPHYs - Application Note
- UNH Test Report

Additional applications notes and information about reference designs using the VSC8244 PHY device can be accessed at the Vitesse Web site.

30 Document History & Notices

Table 61. Document Revision History

Revision Number	Date	Comments
0.2.0	Apr 12 04	• VeriPHY functional changes. Removed Reisters 24E-28E. This feature requires support from an external MCU/CPU and the VeriPHY software library. Contact Vitesse Semiconductor for more information. • Added undocumented pins: C8, M15, R16 to the pin descriptions. Updated JTAG, RESET, SOFT_RESET, TX_CLK_n, EEDAT, EECLK pin descriptions. • Added Section 11.5, 11.6, 12.5, 16, 31.1, 32.3 • Updated Sections 12.3, 12.4, 13, 15, 19, 21, 22, 23.3, 23.4, 24, 25, 26, 26.2, 28.5, 29, 35 • Simplified Register 0-15 descriptions. Clause 37 resiters view was removed from the datasheet to avoid confusion as 1000BASE-X is not supported in this device. • Updated Register 16-18, 22-24, 28-30, 16E, 22E
2.0	June 7 04	• Updated document style to reflect Vitesse corporate standards. • Added Design Guidelines section.
2.1	Aug 4 04	• Removed references to 216 EP-LQFP package option.
4.0	Sep 30 04	• Changed Figures 2 and 19. • Removed Sections 10.1 and 10.2, including Figures 7 and 8. • Updated Sections 13, 14, 15, 17, 17.1, 19.3, 21.1, 23.1, 24.2, 24.4, 24.5, 24.6, 24.32, 25.2, 25.5, 25.6.1, 25.6.2, 25.6.3, 25.7.1, 25.7.2, 29.1. • Added Sections 25.8.9 and 26.2.
4.1	June 2006	• Added ordering information for lead(Pb)-free products. For more information, see Section 27: "Ordering Information". Also, for the MSL rating of the lead(Pb)-free products, see Section 26.2: "Package Moisture Sensitivity".

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